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Optimal design of a low-power, phase-switching modulator for implantable medical applications

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ABSTRACT

Since first proposed in JSSC [1], phase-switching modulation has been proved to be a viable transmission scheme. In this paper, we explored the maximum data-rate of phase-switching modulation and proposed a modified quadrature oscillator with a self-bias circuit to isolate the disturbance in power supply and ground. Dividers and filter are also optimized to minimize parasitic resistor and capacitor. The prototype is fabricated in a 0.18 μm CMOS process, with an active chip area of about 0.13 mm × 0.35 mm. The total power consumption of the modulator is only 2 mW with an energy efficiency of 80 pJ/Bit. This modulator has been successfully embedded in a direct-up conversion transmitter for medical application.

1. Introduction

Implantable Medical Device (IMD) may carry wireless communication and enable on-line monitoring and treatment without additional surgical procedures [2]. Such devices can also be deployed by healthcare systems to provide 24-h health alarm, which is especially crucial for an aging society [3,4].

In an IMD communication system, the transceiver receives simple commands to control its operation and transmit high volume of physiological data, including both multimedia and photo data [5,6]. On the other hand, the receiver does not have stringent design constraints and hence is designed with fewer control bits and slower data rate [5,6]. Thus, the data communication of IMD is typically asymmetrical with only transceiver demanding wide bandwidth [5]. For example, for an 8-bit 256 × 256-pixel color image with 10 fps (frames/sec) and 5:1 image compression ratio [6], the required transmission data rate is up to 3.15 Mbps, as calculated in Eq. (1).

$$Data\ \ Rate = \frac{bits\_num \times pixel \times fps \times 3(RGB)}{compression\_ratio} \quad (1)$$

In general, IMD utilizes the human body as the media to transmit and exchange information. The output power of the transmitter is therefore limited to avoid heat damages to human body. Since the transmitter dominates the total power budget, low power and high efficiency transmitters are then highly desired for IMD communication systems [2–6]. Since the high sampling clock is almost beyond the digital circuit's capacity, most prior works are based on analog implementations [7,8].

As in prior works [3,6,9–13], the modulation schemes of frequency-shift-keying (FSK) and on-off-keying (OOK) are widely used in IMDs. Since OOK is strongly susceptible to interference, a linear power amplifier (PA) is also required. In order to reduce the energy consumption and system cost, most prior works utilize an injection-locked signal to replace the crystal oscillator. However, there is an implicit constraint for ILO, whose narrow locking bandwidth suggests that it can only operate at a fixed frequency. Moreover, two large on-chip inductors as required by the design are not ideal for implantable devices.

There are two common architectures of analog FSK/PSK modulators. One is based on VCO direct modulating [12–14], while the other is based on divide ratio tuning [15–17]. For VCO direct modulating topology, the modulation is realized by directly varying the control voltage of VCO, thereby reducing power consumption and design complexity. However, the output frequency may drift from its desired value due to the PLL open loop, which ultimately degrades the modulation spectrum. For divide ratio tuning topology, it may achieve a high precision frequency resolution with low in-band noise at the cost of complex topology, thereby resulting in significant energy consumption per bit. Moreover, its data rate is limited by the PLL bandwidth and hence can be only used in low

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data rate applications.

In order to tackle the aforementioned challenges and further reduce power consumption, one viable solution is to conduct modulation outside PLL, which is so-called phase-switching modulation as proposed in Ref. [1]. The solution is featured with simplicity and semi-digital nature, thereby achieving higher transmission efficiency in comparison to prior works [11–13]. However, there is not much discussions in the prior work [1] on design optimization to achieve trade off among power, area, data-rate and energy efficiency. Moreover, the use of on-chip inductor also prevents the full integration and wider adoption of the proposal. This paper addresses the limitations in Ref. [1] and demonstrates a novel fully integrated optimal phase-switching modulator with maximized data rate. The major contributions of the work include:

- We present the system design of a phase-switching modulator with maximized data rate.
- We proposed a modified quadrature oscillator with a self-bias circuit to isolate the disturbance in power supply and ground.
- We investigated the designs for divider and filter to explore its design space and achieve optimal performance.

The paper is organized as follows. In Section 2, we reviewed background and prior works. Then the system architecture is introduced and key building blocks are discussed in Section 3, including the analysis and optimization methodology details. Finally, Section 4 and 5 present the experiment results and the conclusions.

2. Background

Fig. 1 illustrates two widely used architectures of FSK modulators. For divide ratio tuning topology in Fig. 1. (a), the input data is injected into the divider through filter, resulting in frequency deviation by instantly changing the divider ratio. This topology is only suitable for narrow band data transmission, as the data rate is limited by the PLL bandwidth, which is usually less than 1 MHz [14]. An equalizer can be inserted to enhance the data rate beyond loop bandwidth, but the gain error of the equalizer would further degrade the FSK performance [15].

In order to eliminate the data rate limit, a VCO direct modulation, as shown in Fig. 1. (b), can be applied. The modulation occurs outside the closed-loop PLL. Thus, the topology does not suffer from PLL bandwidth limitation, resulting in higher data rate. However, the output frequency may drift from the desired value due to the PLL open loop. Moreover, the modulation spectrum is sensitive to VCO gain, and hence leads to modulation inaccuracy.

Unlike the two architectures, phase-switching modulation is conducted outside PLL. For a modulated FSK signal, a signal can be written as shown in Eq. (2), where A_m is the amplitude, f_c is the carrier frequency, and Δf is frequency deviation. The signal can be further rewritten as in the second line in Eq. (2), where β is a modulation index, T_b is the bit period and $\beta = 2\Delta f \times T_b$.

$$\begin{aligned} x_{FM}(t) &= A_m \cos(2\pi f_c t + 2\pi \Delta f t) \\ &= A_m \cos\left(2\pi f_c t + \beta\pi \frac{t}{T_b}\right) \end{aligned} \tag{2}$$

The basic idea of FSK is to modulate the input data into carrier's frequency. In Eq. (2), FSK modulation will result in a PSK modulation at the same time, *i.e.* the phase will change by $\beta\pi$ in one data period. Thus, it is hard to distinguish FSK modulation from PSK modulation. A conceptual diagram of phase-switching modulation is demonstrated in Fig. 2. (a). In the figure, when $b = 0$, the modulated signal $S_{FSK}(t)$ is as in Eq. (3); when $b = 1$, the modulated signal $S_{FSK}(t)$ changes as in Eq. (4). In the equations, f_c is the carrier frequency, f_d is the deviation frequency.

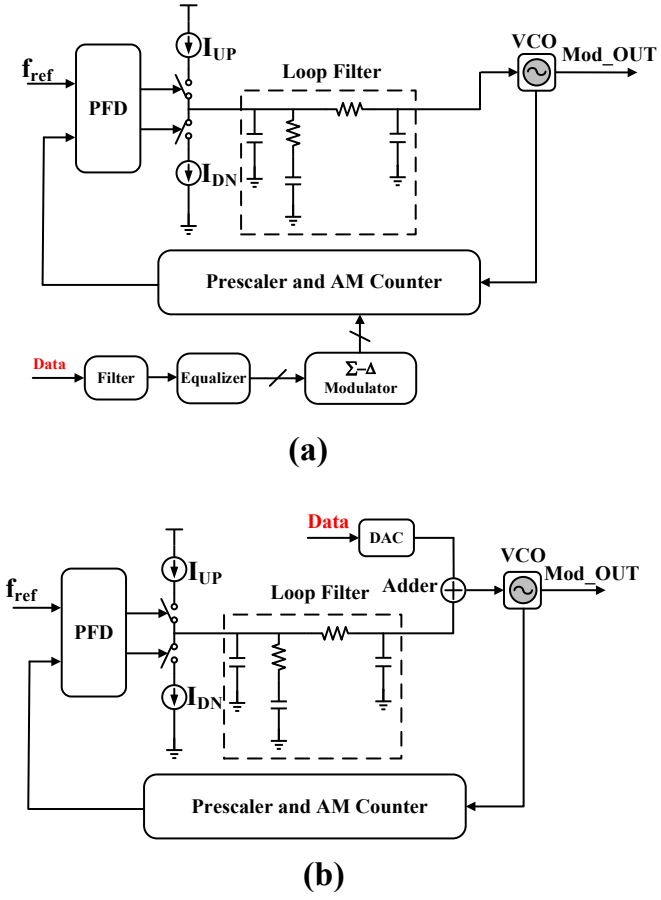

Fig. 1. Two modulator architectures: (a). Divide ratio tuning (b). VCO direct modulating.

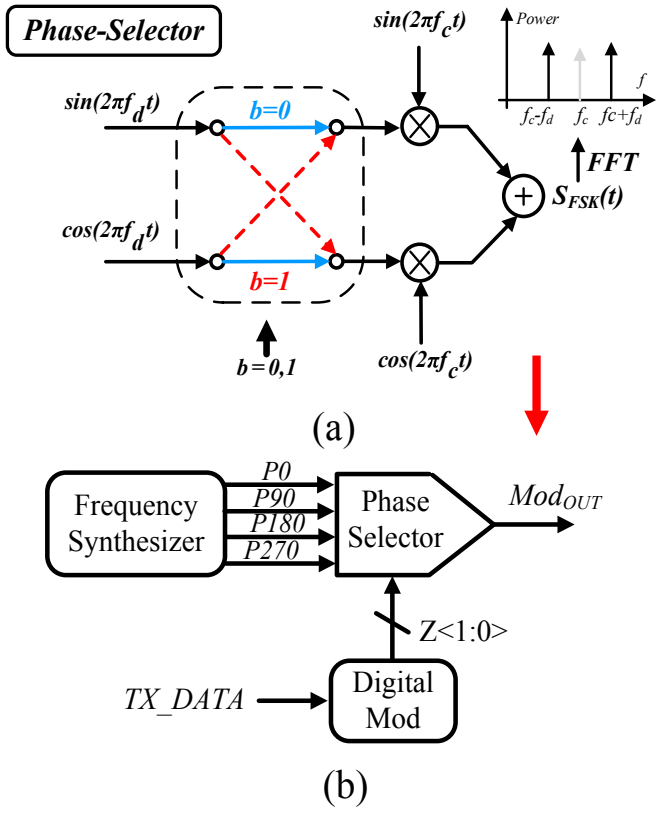

Fig. 2. (a). Conception diagram of modulation operating principle (b). The system architecture.

$$S_{FSK}(t) = sin(2\pi f_c t) \cdot sin(2\pi f_d t) + cos(2\pi f_c t) \cdot cos(2\pi f_d t) = cos(2\pi f_c t - 2\pi f_d t) \quad (3)$$

$$S_{FSK}(t) = cos(2\pi f_c t) \cdot sin(2\pi f_d t) + cos(2\pi f_d t) \cdot sin(2\pi f_c t) = sin(2\pi f_c t + 2\pi f_d t) \quad (4)$$

$$sin(2\pi f_c t + 2\pi f_d t) = cos(2\pi f_c t + 2\pi f_d t - \pi/2) \quad (5)$$

With Eq. (4) rewritten as Eq. (5), Eq. (3) and Eq. (5) represent negative frequency deviation and positive frequency deviation, respectively. In phase-switching modulation, the quadrature signals change their channel paths according to the input data. Then the signals are multiplied by another pair of quadrature signals acting as a mixer, which results in the system architecture as shown in Fig. 2. (b).

3. Phase switching modulator design and optimization

3.1. Overview of phase switching modulator

As discussed in the last section, for phase switching modulator, its baseband signal directly controls the desired quadrature phase. Thus, we can deploy the following circuit implementation as in Fig. 3, which consists of 4 parts. First, an integer-N frequency synthesizer is used to provide 4 quadrature signals for IQ channels. Then a low power ring-based quadrature oscillator with self-bias is adopted to improve phase noise performance. An injection-locked frequency divider (ILFD) is used as a pre-scaler for low power operations. Finally, a frequency band selector enables two ultra-high frequency bands operation.

One core part of the design is the Gilbert-cell based phase selector which achieves both phase switching and frequency multiplication. An on-chip balun follows the modulator to support full voltage swing for noise suppression. Fig. 4 displays the system simulation result of the modulator. The output spectrum is spread from 750 MHz to 850 MHz. From Fig. 2(a) and Eqs. (3)~(5), we know that the frequency deviation is equivalent to the data rate, which is 1 Mb/s in our case here. The output power can then be as high as −17 dBm. Moreover simulation results show that the spectrum is smooth with narrow main lobe and rapidly decreasing side-lobe energy.

3.2. Quadrature oscillator

The block-level diagram of the proposed quadrature oscillator and the circuit implementation of a delay cell are illustrated in Fig. 5 [18]. It is noted that neither on-chip nor off-chip inductors are used in this oscillator to reduce area and cost overhead. The core of the circuit is two cross-coupled inverters. The NMOS transistors M_1 and M_2 form the input pair to increase the transconductance for high frequency operation. The two cross-coupled PMOS transistors M_3 and M_4 provide the negative resistance and positive feedback for oscillation. The tuning is achieved by adjusting the gate voltage of PMOS transistors M_5 and M_6, while diode-connected transistors M_7 and M_8 serve as a load for the input. The outputs of the oscillator are added to PMOS transistor M_9 and M_{10} to improve linearity. They acts as single transistor transmission gate, so we can neglect the on-state resistors for simplification during small signal analysis. The bias works in near-threshold region to reduce the power consumption.

The equivalent half-circuit of the proposed oscillator is shown in Fig. 6. The tail resistance is doubled according to common source point. The open loop gain of the oscillator is calculated by Eq. (6), where g_{m1}, g_{m3}, g_{m5} and g_{m7} are transconductance of transistor M_1, M_3, M_5 and M_7, respectively. r_{O3} is the output resistance of transistor M_3. R is the equivalent resistance of bias transistor. If channel-length modulation index is negligible, and r_{O3} approximates to infinity, then Eq. (6) can be simplified to Eq. (7).

$$A_V = -\frac{g_{m1}}{1+2g_{m1}R}\left(\frac{1}{g_{m5}} \parallel \frac{1}{g_{m7}} \parallel r_{O3} \parallel \frac{-1}{g_{m3}}\right) \quad (6)$$

$$A_V = \frac{g_{m1}}{1+2g_{m1}R}\left(\frac{1}{g_{m5}+g_{m7}-g_{m3}}\right) \quad (7)$$

According to Barkhausen criteria, when the total phase shift around

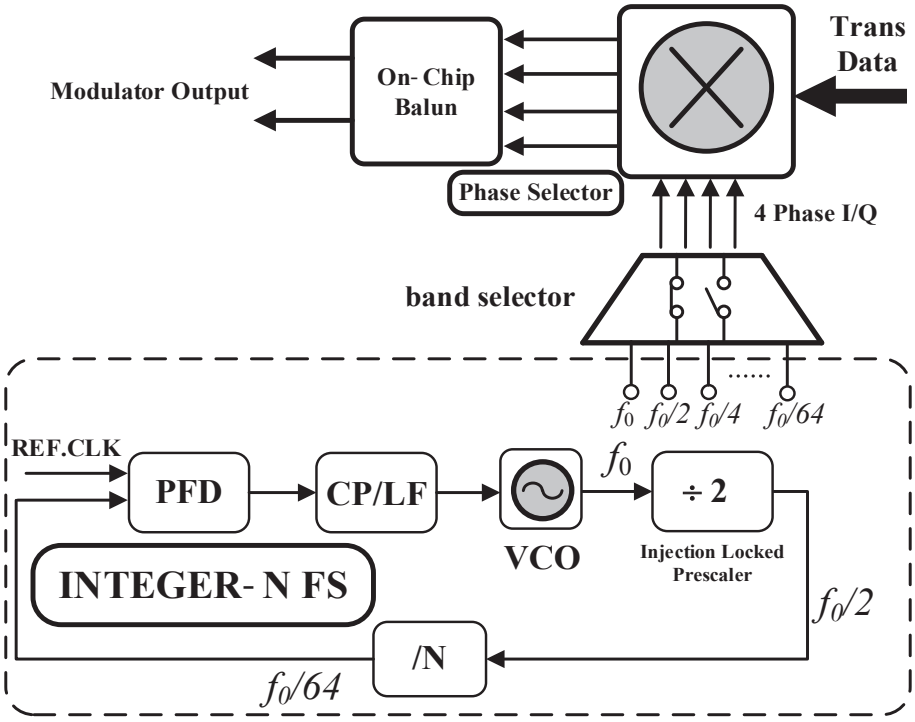

Fig. 3. Block diagram of the modulation circuit implementation.

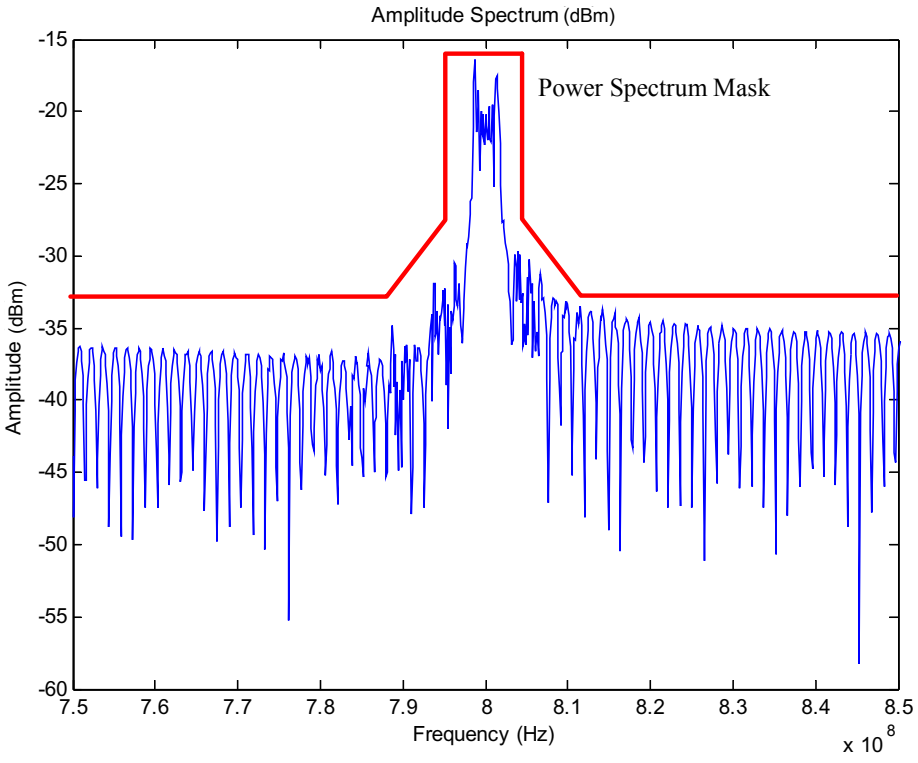

Fig. 4. Output spectrum of the modulator.

the closed loop reaches 360° and the gain is greater than unity, then the circuit oscillates. The oscillation frequency is given by Eq. (8), where R_{eq} is the equivalent output resistance and C_L is the equivalent output capacitance of the delay cell.

$$F_{OSC} = \frac{1}{2NR_{eq}C_L} \tag{8}$$

It is also noted that for the equivalent half-circuit, R_{eq} is approximately equal to $r_{O1}//r_{O3}//r_{O5}//r_{O7}$, where r_{Oi} $(i = 1, 3, 5, 7)$ is the output resistance of each transistor. By neglecting r_{O1}, r_{O3} and r_{O7}, then R_{eq} is approximately equal to r_{O5}, which is given by Eq. (9), where λ, μC_{ox} and V_T are channel-length modulation index, process parameter and threshold voltage respectively.

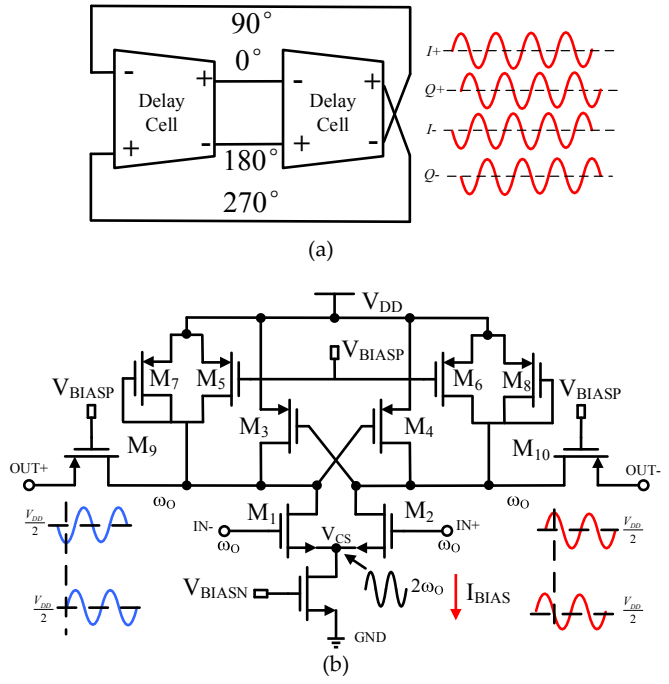

Fig. 5. Proposed quadrature oscillator (a). Block-level diagram of the proposed quadrature oscillator (b). Circuit implementation of delay cell.

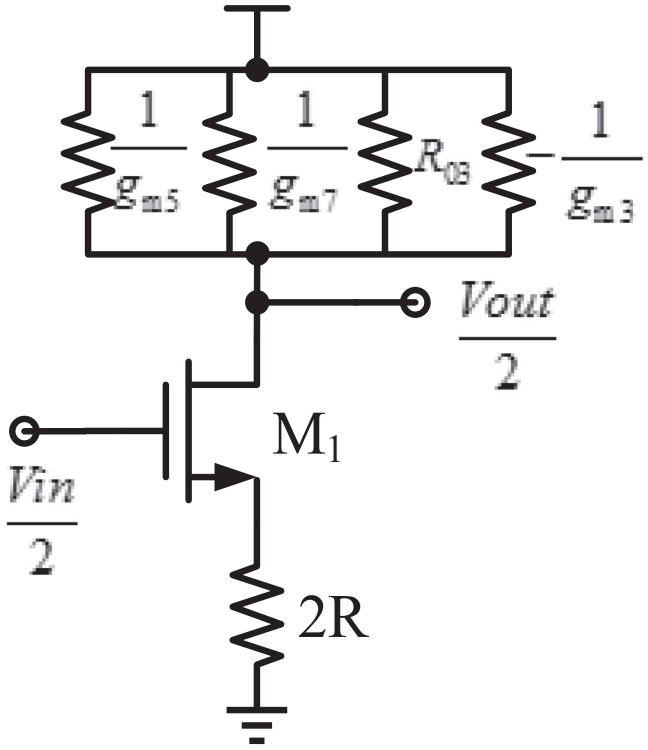

Fig. 6. Equivalent half-circuit of the proposed oscillator.

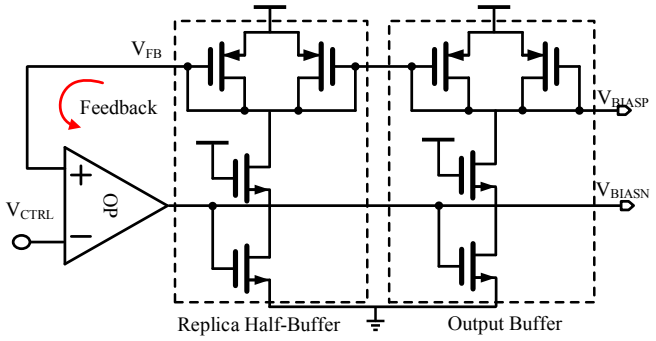

Fig. 7. The architecture of self-bias circuit.

$$r_O = \frac{\partial V_{DS}}{\partial I_D} = \frac{1}{\partial I_D / \partial V_{DS}} = \left[\lambda \cdot \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{CTRL} - V_{DD} - V_T)^2\right]^{-1} \quad (9)$$

With the discussion and formulation above, it is clear that the oscillation frequency varies with changing the value of r_{O5}. In other words, when control voltage increases, the drain current of transistor M_5 decreases and r_{O5} increases, thereby resulting in decreasing oscillation frequency.

The noise of this quadrature oscillator mainly comes from the disturbance of power supply and ground. For example, when a MOS transistor in the digital part turns on and charges the load capacitor, an instant current pulse is generated in the ground. This pulse then flows through the inductive wire and induces a voltage bounce on ground. Eventually this noise can be coupled through the substrate to the analog part. If the circuit is immune to such disturbance, the noise performance of the oscillator can be greatly improved. Here is a self-bias circuit proposed to isolate the noises in power supply and ground, as demonstrated in Fig. 7.

The self-bias circuit is designed with a differential amplifier and feedback buffer stages. This self-bias circuit is used to generate I_{BIAS}, and the replica half buffer stage translates this current to V_{CTRL} through the diode-connected device. The feedback amplifier adjusts the bias current I_{BIAS} accordingly to have the voltage swing of the buffer equal to V_{DD}-V_{CTRL}. Thus, this technique may dynamically adjust the bias current in each buffer stage to maintain the following equality V_{DD}-V_{CTRL}= $I_{BIAS} \times R_{LOAD}$, thereby preventing process variation and noise disturbance.

3.3. ILFD

ILFD is based on the principle of locking a low frequency oscillator to an incoming signal at its 2nd harmonic. When operating at a frequency two times lower than the VCO, ILFD consumes significantly less power than their digital counterpart. Most recently-reported ILFDs are based on either on-chip LC oscillator or ring oscillator. Since on-chip spiral inductor often consumes a large silicon area, LC oscillators based ILFD is then not good solution for the sub-GHz IMD applications. We therefore

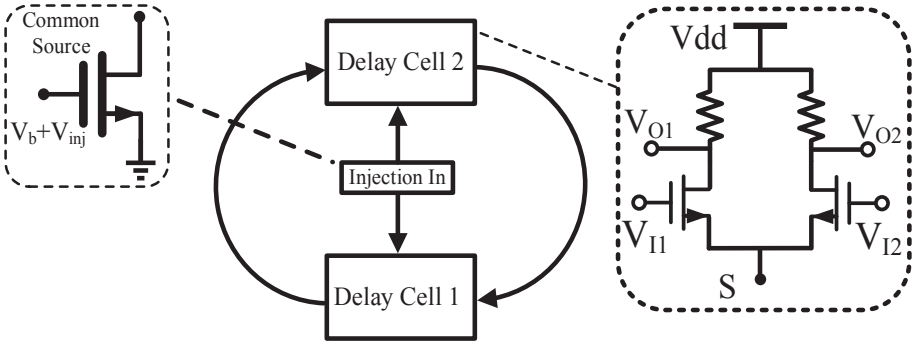

Fig. 8. Injection-locked frequency pre-scaler.

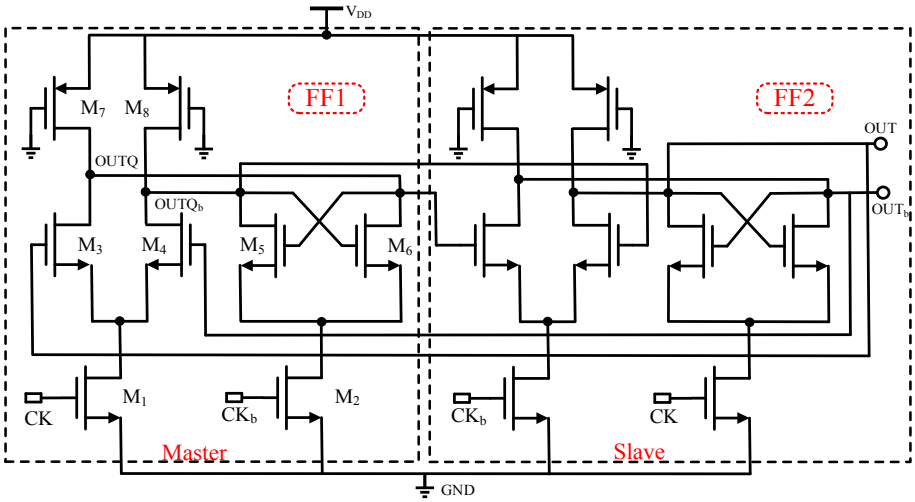

Fig. 9. Current mode logic frequency divider.

adopt the ring oscillator topology here.

In general, the first stage frequency divider within the frequency synthesizer consumes significant power. It is then necessary to introduce a low power divider as a pre-scaler. So that the subsequent digital dividers do not need to operate at the full RF frequency, thereby reducing the total power consumption of the frequency synthesizer. An ultra-low power ILFD is used here as a pre-scaler to prevent the subsequent digital dividers from operating at high frequency [19]. The ILFD is plotted in Fig. 8, where the injection signals with bias are at the common source point. The ILFD is based on a 2-stage differential ring oscillator, with the free running oscillation pulled to an adjacent frequency f_o by injecting a periodic current of frequency $2f_o$. The two delay cells are the same consisting of two NMOS transistors with the aspect ratio of 5μm/0.18 μm. The aspect ratio of injection transistor is chosen to be 2 μm/1 μm with the trade-off between injection strength, bias current and parasitic capacitance. In order to maintain the frequency lock, the loop should have a gain of 1 and the phase shift of π from Cell 1 to Cell 2.

3.4. CML frequency divider

There are several techniques such as injection locking [20,21] and Miller divider [22,23] that are used in high speed frequency dividers. Compared with them, a CML based divider has a much wider operating range, especially with narrow locking range of ILFDs. A CML frequency divider is proposed in Fig. 9 using two master-slave flip-flops. The master and slave stages consist of an input stage ($M_{1,\ 3,\ 4}$), a load stage ($M_{7,\ 8}$) and a latch stage ($M_{2,\ 5,\ 6}$). The current sources in the conventional CML latches are omitted for low voltage operation.

When the inputs CK and CK_b are equal to the common mode value, the divider becomes a quadrature oscillator whose oscillation frequency is determined by output parasitic parameters. If the delay from the gate to the drain of M_3 is τ_{pd}, then the oscillation period is equal to $4\tau_{pd}$. Thus, the circuit oscillates at $1/(4\tau_{pd})$ and the signal at the drain of M_3 lags the one at the gate by 90°. In general, the higher self-oscillation frequency leads to higher operating frequency for dividers. Moreover, the oscillation frequency strongly depends on the transistors size. Fig. 10 shows the simulated oscillation frequency as function of the width of latch transistors ($M_{5,\ 6}$) for varying widths of PMOS loads ($M_{7,\ 8}$). In the simulation, the widths of $M_{3,\ 4}$ are 0.8 μm; $M_{1,\ 2}$ are 0.4 μm; lengths of all the transistors are 0.18 μm. As seen in the figure, for a given load, wider latch or smaller load leads to lower frequency, as R_L increases with smaller loads. Though the capacitance C_L also decreases, it decreases at a slower rate than the increase of R_L. Since the power consumption is linearly proportional to the operating frequency, the ratio sizes of latch transistors and load transistors are chosen to be 1/0.18 and 1.44/0.18, for the trade-off between area and power. In the proposed PLL system, a five stages CML divider is used as a divider for 32 frequencies.

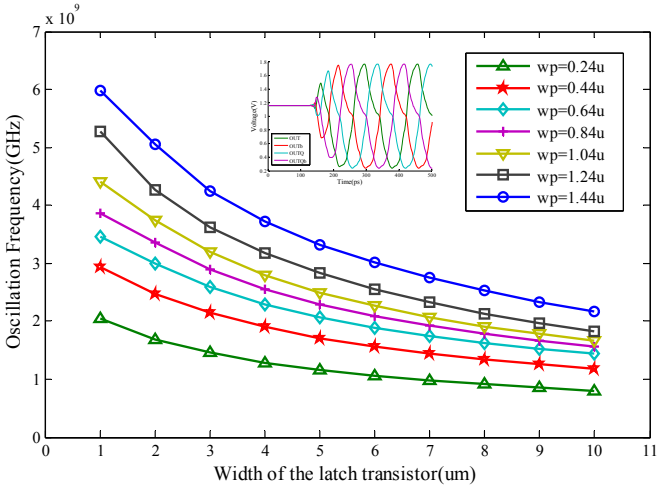

Fig. 10. Maximum operating frequency of CML divider.

3.5. PFD and charge pump

The phase-frequency detector compares the phase difference between two input signals and produces an error signal proportional to the phase difference. When the phase difference is very small, PFD outputs V_{UP} and V_{DN} will generate narrow pulse, which is not able to activate the charge pump. In order to avoid this dead zone problem, a delay stage is inserted to the reset path. The logical implementation of this PFD is plotted in Fig. 11 using two edge triggered single-phase-clock (TSPC) DFFs and a NOR gate for the reset signal, where the circuit implementations of TSPC and NOR are shown in Fig. 12. The charge pump (CP) can be modeled as a current source with two switches that are controlled by the PFD. The two switches decide whether the CP draws current from or sends current into the loop filter, as shown in Fig. 13, in which high swing cascade current mirrors are used to achieve both high output impedance and large output swing. An odd stages delay chain is also used to minimize delay mismatch. Simulation results in Fig. 13 show the cases when the reference leads or lags the divided output by 45°.

3.6. Second order loop filter

The PLL applies a second-order loop filter for small reference spurs, as shown in Fig. 14. Capacitor C_1 is acceded to filter high frequency ripples. The impedance of the 2nd order loop filter is represented by Eq. (10).

$$Z_{LPF,2^{nd}}(s) = \frac{1 + R_2C_2 \cdot s}{R_2C_2C_1 \cdot s^2 + (C_1 + C_2) \cdot s} = \frac{1}{s} \cdot \frac{1}{C_{tot}} \cdot \frac{1 + s/\omega_z}{1 + s/\omega_p} \tag{10}$$

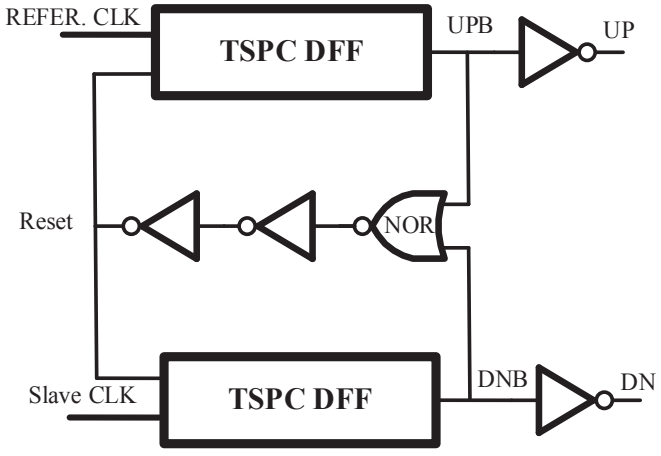

Fig. 11. PFD circuit implementation.

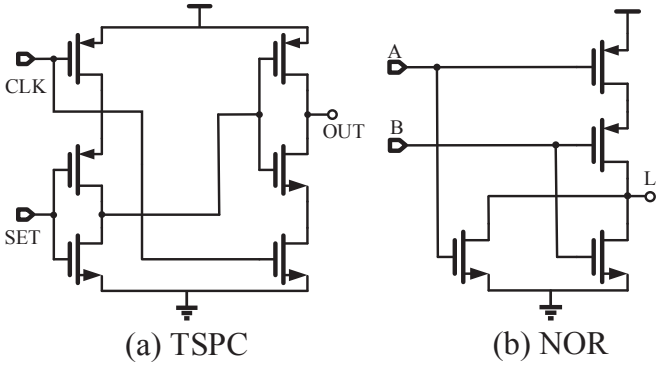

Fig. 12. TSPC and NOR circuit implementation.

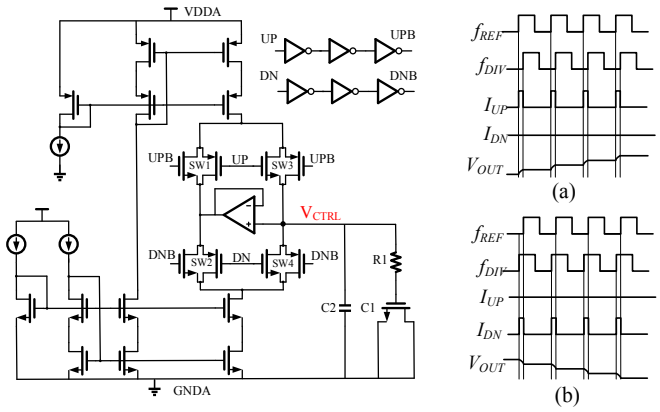

Fig. 13. Charge pump implementation with the simulation results of the reference (a) leads and (b) lags the divided output by 45°.

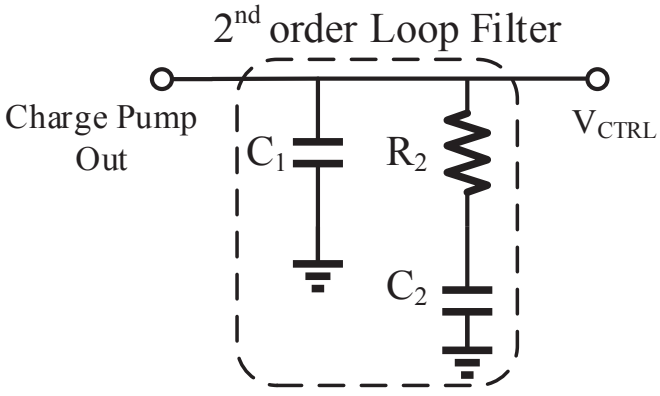

Fig. 14. The 2nd loop filter.

where the pole and zero are given by Eq. (11) and Eq. (12), and C_{tot} is defined by Eq. (13).

$$\omega_z = 1/R_2C_2 \tag{11}$$

$$\omega_p = C_{tot}/R_2C_2C_1 \tag{12}$$

$$C_{tot} = (C_1 + C_2) \tag{13}$$

In general, $C_1 \ll C_2$. When the filter works in low frequency, the output impedance is $1/sC_{tot}$. On the other hand, when the filter works in low frequency, the output impedance changes to $1/sC_1$. In order to save area, MOS capacitors are used in our design. The simulation setup of various

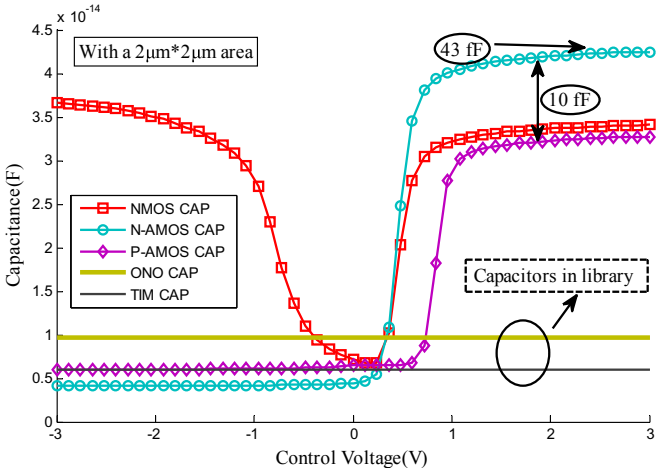

Fig. 16. Capacitance of various capacitors.

capacitors is shown in Fig. 15. Various capacitors simulation setup. The simulation results of five different types of capacitors are compared Fig. 16. It is clear that NMOS transistor in the accumulation mode shows the highest capacitance per unit area.

Since transistor-level frequency simulation using Cadence Spectre is very time-consuming, instead we conduct extensive system level stability analysis in Matlab Simulink. The simulation results for the methodology discussed in the last few subsections are shown in Fig. 17, which proves that the magnitude of the gain decreases linearly with frequency and the phase margin is over 60°. The transistor-level simulation of the PLL startup is depicted in Fig. 18. With 500 kHz bandwidth of the PLL, the settling time of the PLL is less than 6 μs.

The phase switching circuit (also known as phase selector) can deliver IQ-channel signals from PLL to the up-convert paths. The circuit diagram of the proposed phase selector is shown in Fig. 19, which consists of a gm-stage and digital switches controlled by quadrature signals and baseband signal. The baseband stages can be viewed as digital switches, whose large swing facilitates the operating speed. Compared with the traditional Gilbert-cell mixer, there is only one current source in the design and the mismatches between IQ channels are automatically eliminated.

With the proposed design it is easier to complete the modulation as the baseband signal directly controls the desired quadrature phase. The output of the proposed phase selector is plotted in Fig. 20, where I+, I-, Q+, Q- are quadrature signals from PLL. When DATA is 0, the Q+ is passed through; when DATA is 1, the input signals change their order and I+ is passed through. As signal 5 and signal 6 in the plot are out of phase, an on-chip balun following the phase selector is used to achieve signal conversion. The baseband determines how the input phases are

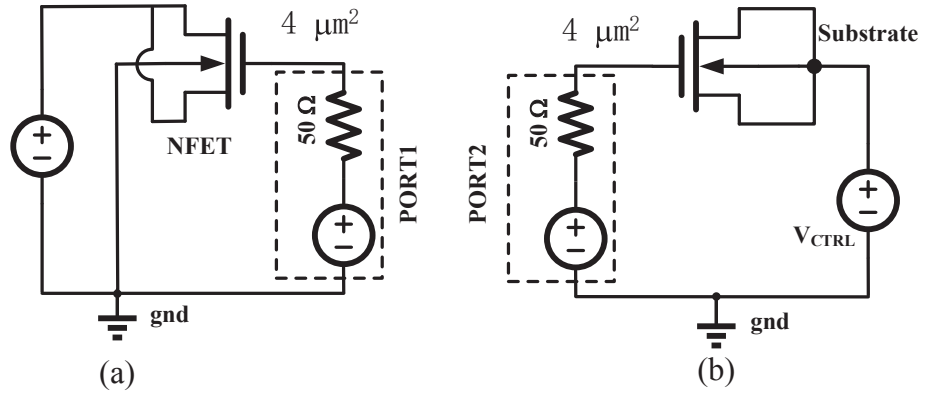

Fig. 15. Various capacitors simulation setup.

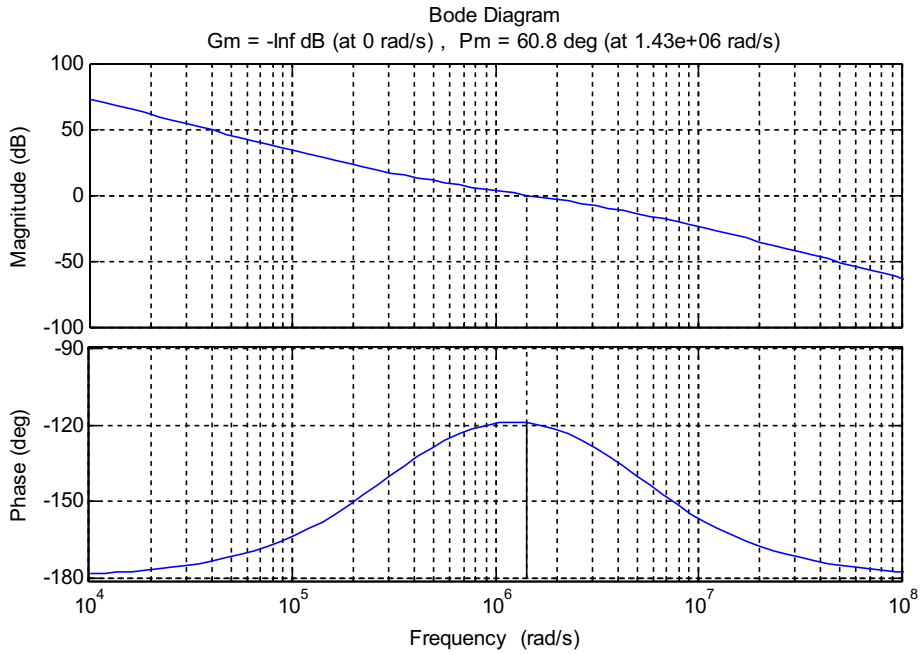

Fig. 17. Open loop AC response.

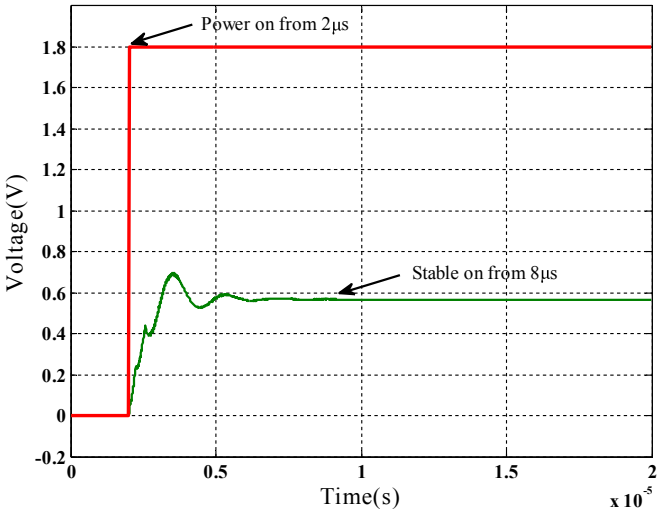

Fig. 18. Transistor-level simulation of the PLL startup.

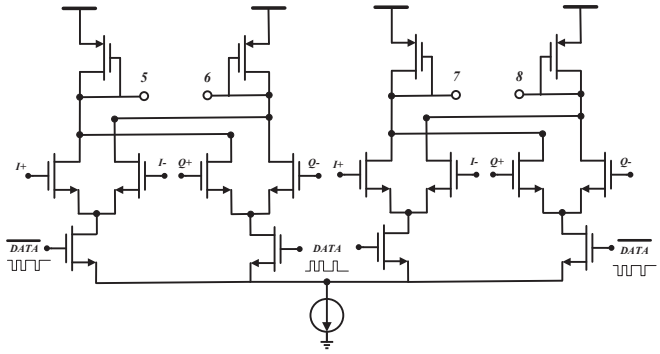

Fig. 19. Circuit diagram of phase switching.

combined in the phase selector. The maximum data rate is then determined by the parasitic capacitor and resistor of the digital switches. In order to increase data rate, the parasitic capacitor and resistor should be as small as possible in the signal path. When the data rate of baseband is *N* times of the period of quadrature signals, it exhibits a QPSK modulation. Such constant envelope feature of the proposed modulator is desired for efficient nonlinear power amplifier.

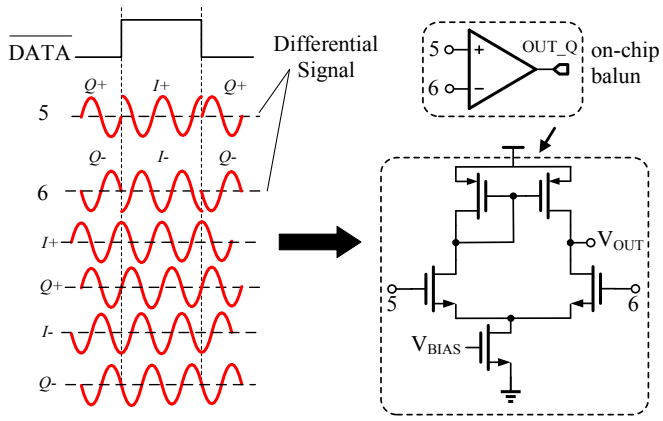

Fig. 20. The output of the phase selector.

4. Experimental results

4.1. Experimental setup

The prototype was fabricated in a UMC 180 nm CMOS technology with 4 Aluminum interconnect layers. The chip layout is presented in Fig. 21. (a), with its die photo of two major modules in Fig. 21. (b). The chip size is 0.85 mm × 0.75 mm, which is determined by the ESD-protection pads. Thanks to the design without on-chip inductor, the active chip area is only 0.12 mm × 0.35 mm. The die was wire-bonded to an FR4 printed circuit board (PCB). Fig. 22 shows the PCB design of the work, with the chip encapsulated in a 3 mm × 3 mm quad flat non-leaded (QFN) package. The signals in the chip were all terminated by SMA

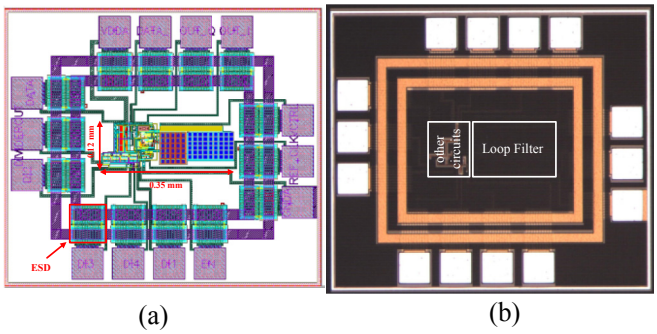

Fig. 21. (a) Chip layout (b) Chip die photo.

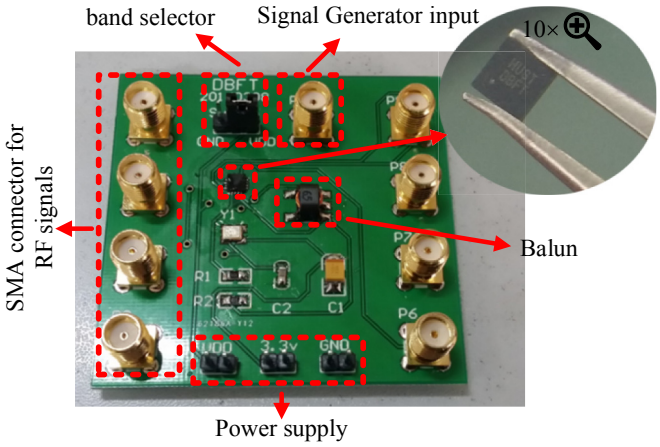

Fig. 22. PCB of the modulator.

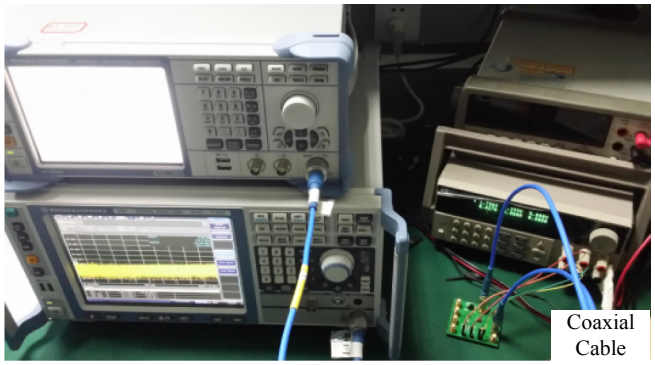

Fig. 23. Chip measurement setup.

connectors with 50 Ω characteristic impedance. The frequency band selector is implemented by a jumper cap. The data rate is measured by feeding the input data to a TOKO B5F type Balun, which converts the single ended input to a differential signal. The measurement setup of RF signals is pictured in Fig. 23, with an IT6322A DC power supply providing two supply voltages, 1.8 V for the chip and 3.3 V for the 15.625 MHz crystal oscillator. The data input is combined with an SMA and connects Rohde & Schwarz SMBV 100 V Signal Generator to generate the transmitting data. All RF signals are analyzed by Rohde & Schwarz FSV Signal Analyzer through coaxial cables.

4.2. Performance measurement

The measured phase noise of the free running oscillator is illustrated in Fig. 24, which achieves −108.45 dBc/Hz at 1 MHz offset with a center

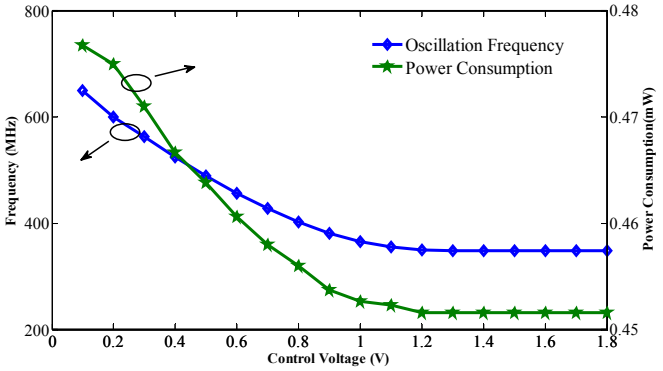

Fig. 25. Measured tuning range and power consumption against control voltage.

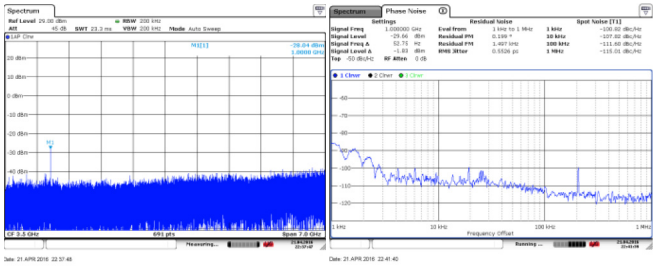

Fig. 26. Spectrum and phase noise of the PLL.

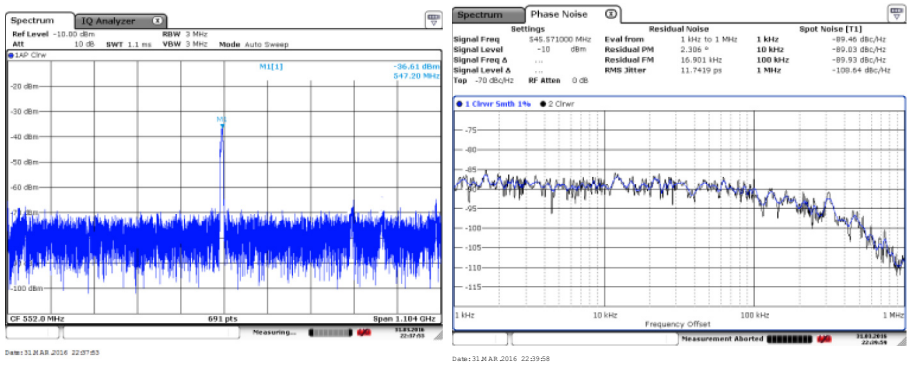

Fig. 24. Spectrum and phase noise of the free running oscillator.

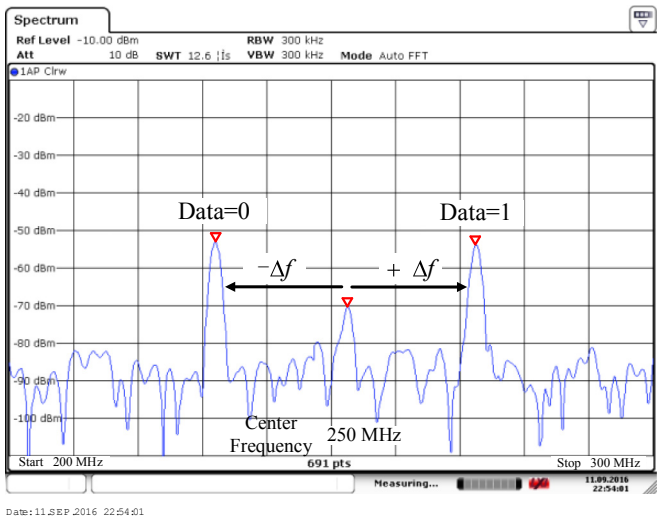

Fig. 27. The spectrum of modulator output at 25 Mb/s input.

frequency of 540 MHz. The use of self-bias circuit alleviates much of the phase noise contributed by the power supply. Since supply or substrate noise is the dominant noise source for this system, the proposed quadrature oscillator achieves a very low phase noise.

The tuning range and power consumption are shown in Fig. 25. The oscillator has a tuning range of 340 MHz from 349 MHz to 689 MHz when the tuning voltage is varied from 0 to 1.1 V. As shown in Fig. 25, when the control voltage is larger than 1.1 V, the tuning PMOS transistor will be turned off. Then the oscillator frequency will be reduced to its minimum without further changes. The gain of oscillator is nearly 0.309 MHz/mV when control voltage is within the range of 0–1.1 V. Fig. 25 also shows that the power consumption is linearly proportional to the oscillation frequency and the power consumption is merely 453 µW at 0.9 V control voltage.

The close-in phase noise is mainly contributed by the frequency synthesizer. It results in a rotation of the modulation constellation, thus degrading the Error Vector Magnitude (EVM) [3]. Fig. 26(a) shows the spectrum of the local oscillator with a frequency span of 7 GHz. The PLL achieves a stable carrier frequency 64 times of the reference frequency and the reference spur level is suppressed to out of band. Without off-chip bias-Tee, the output power is −29.6 dBm with a center carrier frequency of 1 GHz. Fig. 26(b) shows the measured PLL phase noise as a function of the frequency offset with 0.5526 ps RMS jitter. The phase noises are −100.82 dBc/Hz and −115 dBc/Hz at offset frequency of 1 KHz and 1 MHz, respectively. By applying a 25 Mbps bit stream to the input of modulator, the output signal is shown in Fig. 27. The output spectrum is spread from 200 MHz to 300 MHz. As discussed in Eq.(3)–(5), the frequency shift in the carrier frequency is the change of the input data stream. The carrier frequency is one eighth of the LO, and modulated signal forms two sideband around 250 MHz with power of −53 dBm and −55 dBm, respectively. When operating under a 1.8 V supply, the modulator only consumes 1 mA current at maximum data rate.

The interface issues in the test setup as well as cross-talk and unwanted tones in the vicinity of the desired frequency cause complexity in the measurement such as jitter. In practice, the balun, which is used to provide the external differential signals for the chip, introduces some phase and amplitude discrepancy. The defective differential signals reaching the die will result in a small degradation in the measurement.

4.3. Comparison with existing work

The performance comparison with prior modulator designs is detailed in Table 1. Compared with previous topologies [13–15], the phase-switching modulator exhibits best trade-off in power, data rate and area. As the modulation is conducted outside the PLL, this relaxes the data rate from PLL bandwidth limitation and the data rate can be increased. It also achieves 10 times more energy efficiency than the digital modulation with higher data rate. Compared to the original work in Ref. [1] with an area of 1.17 mm^2, the proposed work can achieve a lower power consumption (4 ×), smaller area (2 ×) and higher energy efficiency (18 ×). This modulator allows easier implementation without the use of on-chip or off-chip inductors. All those features are very appealing for full integration in energy-constrained IMD applications.

5. Conclusions

The power consumption of RF circuits in IMD application is a key challenge to its wider adoption. In this paper, an optimized phase-switching modulator is presented for implantable medical transceivers. The modulator generates modulation signals outside the PLL and eliminate the use power-hungry DACs and filters to achieve low power consumption of 1–2 mW. The maximum data rate is determined by the parasitic capacitor and resistor of the digital switches, which can be higher than traditional schemes. The proposed design was fabricated in a UMC 0.18 µm CMOS process with an active area of 0.13 mm × 0.35 mm and energy efficiency of 80 pJ/Bit. Thus, the design shows appealing features for energy constrained applications such as implanted MICS sensors.

Table 1
Performance comparison with the prior works.

Reference	JSSC [1]	JSSC [3]	JSSC [7]	JSSC [11]	TBiocas [13]	JSSC [14]	TCAS I [15]	This paper
Process	0.18 µm CMOS	90 nm	0.18 µm BiCMOS	0.18 µm CMOS	0.18 µm RF CMOS	0.18 µm CMOS	0.18 µm CMOS	0.18 µm CMOS
Year	2009	2014	2013	2012	2011	2014	2015	2016
Supply	1.4 V	1 V	3.6 V	1 V	1.8 V	0.8 V–1 V	1.8 V	1.8 V
Power	8.8 mW	860 µW	291 µW	2 mW	4.86–9.72 mW	191 µW	57.6 mW	1–2 mW
Modulation	G/FSK	OOK	PPM[a]	FSK	OOK/FSK	OOK/FSK	GMSK	FSK/PSK
Data Rate	6 Mb/s	5 Mb/s	30 kb/s	1 kb/s~10 Mb/s	4/2 Mb/s	5 Mb/s	NA	1–25 Mb/s
Freq. Band	284–435 MHz	2.45 GHz	9.8 GHz	WBAN	2.4 GHz	2.4 GHz	GSM/GPRS	125/250 MHz
Mode	Phase rotator	On-off	Digital	Injection locked	VCO direct tuning	VCO direct tuning	Divide ratio tuning	Phase selecting
Energy Efficiency	1.5 nJ/Bit	172 nJ/Bit	9.7 nJ/Bit	0.24 nJ/Bit	1.2–4.8 nJ/Bit	38 pJ/Bit	NA	80 pJ/Bit @25 Mb/s
Area	1.17 mm^2	1.54 mm^2	2.73 mm^2	4.5 mm^2	1.3 mm^2	0.035 mm^2[b]	4.59 mm^2	0.63 mm^2

[a] Pulse-position modulated.
[b] Core area.

Declarations of interest

None.

Acknowledgement

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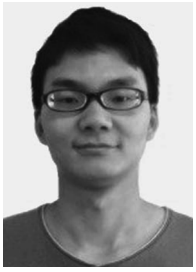

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