Predictive Calculation of Coupling Coefficient Between On-chip Small-area Multilayer Inductors

Xiaowei Xu, Wanghui Zou, Jinran Du, Xiaofei Chen, Xuecheng Zou*

Department of Electronic Science and Technology, Huazhong University of Science and Technology
Wuhan, 430074,China
*e-mail: extxczou@hust.edu.cn

Abstract
A predictive physics-based method for calculating the coupling coefficient between on-chip small-area multilayer inductors is proposed. The new method employs the symmetric approximation and is based on "ring-by-ring" manner, which provides a relatively easy way to estimate the crosstalk between on-chip inductors. The accuracy and effectiveness of the method is evaluated by comparing the calculated values with the electro-magnetic simulation results of a series of inductors with various design parameters. It has been verified that the calculation error of the new method is typically within around 4%.

1. Introduction

On-chip inductors play a significant role in modern CMOS wireless and wireline transceivers, and the small-area multi-layer inductors have the potential to minimize the total chip area and cost, and therefore used intensively in some designs [1], [2]. As the modern integrated circuits achieve an impressively high integration level and become more compact, the crosstalk between on-chip inductors, which is usually represented by the coupling effect, will be a possible limit to the functionality and performance of the circuits. The general method to analyze crosstalk is using electromagnetic (EM) simulation or silicon measurement and extracting coupling coefficient from S-parameters [3]. The obvious disadvantages of EM simulation or measurement are time-consuming and lack of flexibility. In contrast, the Greenhouse method in [4] is an analytical physics-based method and prone to be used to calculate the coupling coefficient in circuit design stage. However, duo to the diversity and complexity of small-area multilayer inductors, it becomes less effective and applicable to use the Greenhouse method directly. Thus, there is a need for fast and accurate methods for the calculation of coupling coefficient. In this paper, a physics-based method employing the symmetric approximation is proposed, and its accuracy and effectiveness is verified by EM simulation.

2. Description of the new method

The coupling effect between inductors manifests itself as mutual inductance M, and the coupling coefficient k reflects the extent of coupling effect, or crosstalk in some scenarios [3]. Assuming the self-inductances of the two inductors are L_1 and L_2, respectively, then the value of k is given by

$$k = \frac{M}{\sqrt{L_1 \times L_2}} \tag{1}$$

Hence, the self- and mutual inductance should be determined first to obtain the value of k.

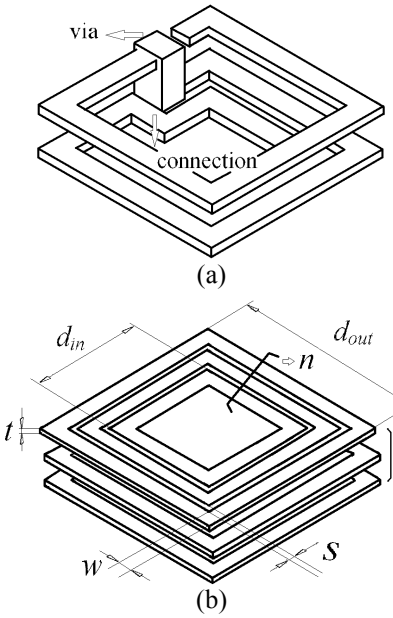

Figure 1. Illustration of the (a) structure of the "real" multilayer inductor and (b) symmetric approximation

2.1 Symmetric approximation

In the Greenhouse method, the self-inductance of straight metal segment and the mutual inductance between metal segments are accurately defined. In principle, all on-chip inductors, including planar and multilayer inductors, can be divided into many straight metal segments, and then the self-inductance of inductor and the mutual inductance between inductors are calculated based on the "segment-by-segment" manner. However, there are many types of on-chip multilayer inductor such as stacked inductors [5], miniature-3D inductors [6] and so forth. Due to the diversity and complexity of the structure, and therefore a large number of metal segments, a specific segment deviation process

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for each inductor and much more calculation steps are often needed. Moreover, as shown in Figure 1(a), there are always vias between metal layers and more metal connections between the inner and outer turns in the "real" multilayer inductors, which makes the segment deviation process more complex and problematic especially for small-area inductors.

In [7], a symmetric approximation method is proposed to derive a closed-form inductance expression for planar inductor. The on-chip inductor is considered as a combination of several concentric closed rings. The symmetric approximation results in regular structure and therefore eases of calculation. In this paper, this scheme is employed for multilayer inductors as shown in Figure 1(b). Obviously, the inter-layer vias and the inter-turn metal connections are omitted under the symmetric approximation. Intuitively, this omission has little impact on accurate for larger-area inductors. However, for small-area cases, this omission may probably result in considerable errors [8]. Furthermore, the difference between various inductor structures will disappear, which seems very strange. The applicability and effectiveness of the scheme for the small-area multilayer inductors will be discussed in detail in section 3.

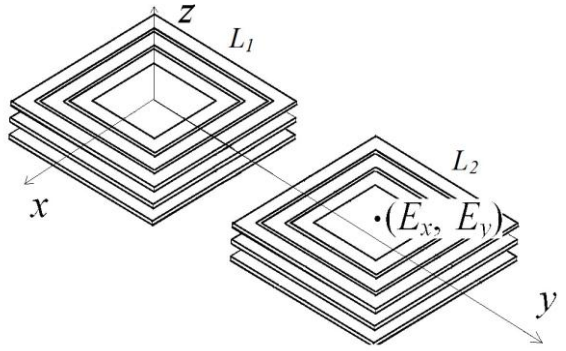


Figure 2. Illustration of two inductors with symmetric approximation. Ez is not shown in the figure.

2.2 Self- and mutual inductance

As shown in Figure 1(b), some inductor parameters are defined: number of layers, l; numbers of turns, n; metal width, w; metal spacing, s; metal thickness, t; outer diameter, d_{out} and inner diameter, d_{in}. Figure 2 shows two inductors with relative coordinate of (E_x, E_y, E_z). E_z means that the two inductors could locate at different chip [2].

Obviously, the new method is based on the "ring-by-ring" manner. Compared with the "segment-by-segment" manner, it reduces calculation complexity dramatically. Hence, the total inductance L of each inductor can be expressed as

$$L = \sum_{i}^{n\times l} L_{self,i} + \sum_{i=1}^{n\times l}\sum_{j=1}^{n\times l} M_{i,j(i\neq j)} \tag{2}$$

where $L_{self,i}$ represents the self-inductance of ring i, and $M_{i,j}$ represents the mutual inductance between ring i and j. The total number of rings of each inductor is $n\times l$. The mutual inductance M between the two inductors can be derived as the summation of the mutual inductance of any two rings between the two inductors and expressed as

$$M = \sum_{i=1}^{n_1\times l_1}\sum_{j=1}^{n_2\times l_2} M_{i,j} \tag{3}$$

where $M_{i,j}$ represents the mutual inductance between ring i of L_1 and ring j of L_2. The expressions for $L_{self,i}$ and $M_{i,j}$ are derived based on the Greenhouse method and used in (2) and (3) repeatedly.

3. Verification

To validate the new method, a series of on-chip small-area multilayer inductors with different design parameters are modeled and simulated in ADS momentum based on 0.18μm 1P6M process. The vias and metal connections are naturally included in ADS models. The values at the frequency of 100MHz are used. Then, the accuracy and effectiveness of the new method is analyzed by comparing the calculated values with the EM simulation results.

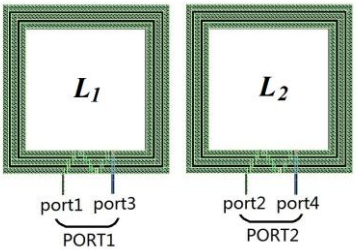


Figure 3. Ports description in ADS Simulation

3.1 EM simulation

As shown in Figure 3, the pair of inductors acts as a four-port device. Because it's usually complicated to extract mutual inductance from four-port S-parameters, the so-called mixed-mode S-parameters are therefore used, which are defined as the S-parameters of differential and common mode between the combined two single-ended ports [2]. In Figure 3, the port 1, 3 and port 2, 4 are combined as PORT1 and PROT2, respectively. The differential and common mode simulations are conducted in ADS with corresponding port settings.

First, the simulated mixed-mode S-parameters need to be transformed into the Y-parameters, the series inductances in differential and common mode are calculated as following

$$L_D = \frac{\mathrm{Im}(-1/Y_{21D})}{\omega},\quad L_C = \frac{\mathrm{Im}(-1/Y_{21C})}{\omega} \tag{4}$$

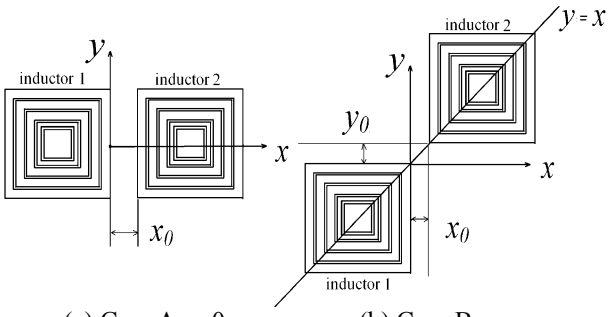
where ω is angular frequency, and the subscripts "D" and "C" represent differential and common mode, respectively. The mutual inductance M is given by

$$M = \begin{cases} (L_C - L_D)/2 & , d_{out1} = d_{out2} \\ (L_D - L_1 - L_2)/2 & , d_{out1} \neq d_{out2} \end{cases} \quad (5)$$

where d_{out1} and d_{out2} are the outer diameters of the two inductors, respectively. The self-inductances L_1 and L_2 need to be determined by separate general two-port simulation. The values of L_1 and L_2 is therefore given by

$$L_1 = \frac{\mathrm{Im}(-1/Y_{11,L1})}{\omega}, \quad L_2 = \frac{\mathrm{Im}(-1/Y_{11,L2})}{\omega} \quad (6)$$

Then, the final value of k is obtained by using (1).



(a) Case A:y=0 (b) Case B: y=x

Figure 4. Two typical cases considered in calculation and simulation

3.2 Results and discussions

Without the loss of generality, two typical cases as shown in Figure 4 are investigated. The design parameters of the pair of inductors vary in each case. In total, over 80 configurations are modeled and analyzed. Figure 5 provides the comparison between the calculated and the simulated values of all samples. The relative errors are also given, which is defined as

$$E_{raletive\_error} = (k_{calculated} - k_{simulated})/k_{simulated} \quad (7)$$

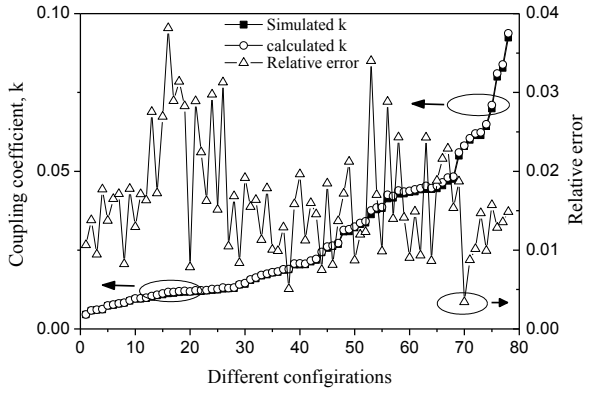
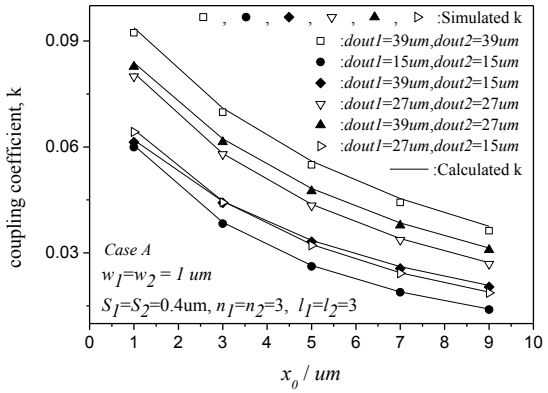


Figure 5. Comparison between the calculated and the simulated values, and the corresponding relative errors

It can be seen that the calculated values agree well with the simulated values. As the value of *k* ranges from 0.005 to 0.094, the maximum relative error is less than 4%, and there is no obvious correlation between the relative error and *k*.



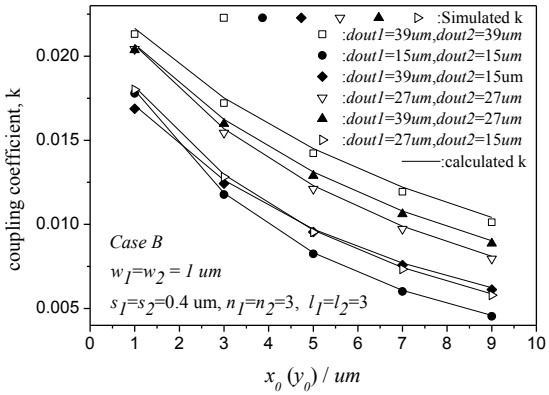


Figure 6. Calculated and simulated values versus inductor spacing

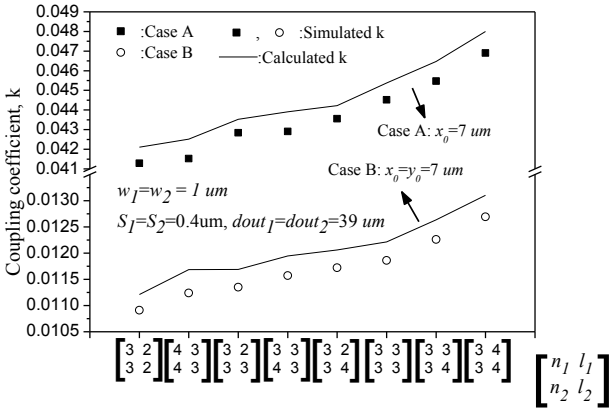


Figure 7. Calculated and simulated values versus number of turns and number of layers

Figure 6 shows the calculated and simulated values versus the spacing between the two inductors in case A and B. As shown in the figure, when the spacing gets larger, the value of *k* drops accordingly, and the calculated values follow the simulated values very well. Figure 7 shows the calculated and simulated values versus number of turns and number of layers in both

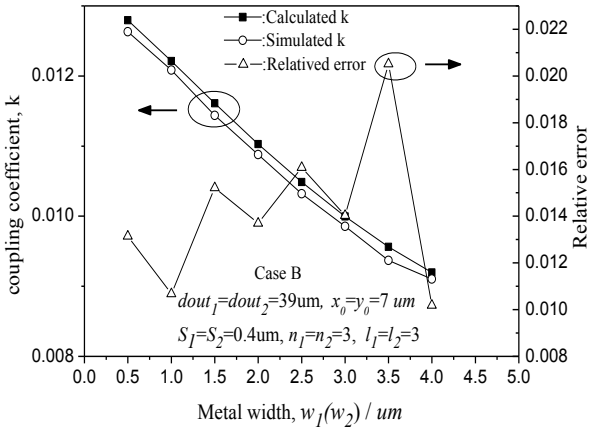


Figure 8. Calculated and simulated values versus metal width, and the corresponding relative errors

cases. The calculated and the simulated values match well also. It can be seen that as the number of turns increase, the value of k decreases, whereas as the number of layers becomes larger, the value of k increases. Figure 8 shows the calculated and simulated values versus metal width in case B, while d_{out} and inductor spacing $x_0(y_0)$ are fixed. The value of k decreases as the metal width increases. The relative errors are also shown in the figure. Further comprehensive analyses find that the value of k is less sensitive to number of layers l, number of turns n and metal width w than to diameter d_{out} and inductor spacing $x_0(y_0)$.

As mentioned before, with the symmetric approximation, the vias and the metal connections may probably contribute to the total error especially for small inductors. However, as shown in the figures, all the calculated values agree with the simulated ones very well, even for small d_{out} of 15μm. Moreover, as shown in figure 5 and 8, it's interesting that the relative errors seem like "random" and show no correlation with k. According to the description in section 2, the calculations of self-inductance L and mutual inductance M are both conducted under the symmetric approximation. Therefore, it's reasonable that the vias and the metal connections have similar impact on the calculation of L and M, and definitely produce errors. However, from (1), when it comes to the calculation of k, the errors in L and M actually counteract to some extent, and eventually the error of k remains within 4% as stated before.

Another issue is the difference between various inductor structures. It should be mentioned that only stacked inductors as in [6] are investigated in this paper. Generally, the stacked inductor has more inter-layer vias and less inter-turn metal connections than miniature 3-D inductor in [7], which results in about the same calculation error for both kinds of inductors. The structure of 3-D solenoid inductor in [3] is similar to that of miniature 3-D inductor. So the new method is believed to be applicable and effective for all kinds of small-area multi-layer inductor on the calculation of k.

4. Summary

This paper proposes a new method for calculating the coupling coefficient of on-chip small-area multilayer inductors. The symmetric approximation and the accompanying "ring-by-ring" manner are able to greatly simplify the calculation process over the conventional "segment-by-segment" manner. It has been proved that the proposed method is accurate and effective to estimate the crosstalk between on-chip inductors, which could be very critical for circuit design. It should be mentioned that the proposed method is actually suitable for inductors located at different chip, though there is not much relative material in this paper.

Acknowledgments

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