# A Quasi-digital QPSK Modulator Design for Biomedical Devices

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For the biomedical transceiver, the data transmission is often asymmetric. At the downlink, the transceiver only needs to receive a simple command to control the operation of the external device, and the receiving data rate is low, about hundreds of Kb/s. However, data collected by external devices such as temperature sensors, pressure sensors, or cameras are often very large, which results in a transmitting data rate of several Mb/s. Therefore, a high energy-efficient modulator is needed. Compared with conventional digital modulator, analog modulator circuits have demonstrated superior energy efficiency at high data rates. This article presents a quasi-digital quadrature phase-shift keying (QPSK) modulator design realized by pure analog circuits which follows a logic design flow. The simulation results show that the system can generate a stable carrier of 64 MHz that meets intra-body communications (IBCs) requirements with a data transmission rate of 10 Mb/s. When the signal-to-noise ratios (SNRs) of the Gaussian channel is 14 dB, it can still maintain a bit error rate (BER) below $10^4$.

CCS Concepts: • **Hardware → Methodologies for EDA**; **Integrated circuits**; **Communication hardware, interfaces and storage;**

Additional Key Words and Phrases: Biomedical, QPSK, analog circuit, modulator

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## 1 INTRODUCTION

With the development of **Complementary Metal-Oxide-Semiconductor** (**CMOS**) technology, chips aimed at real-time monitoring of human physiological signals such as **Electromyogram** (**EMG**), **Electrooculography** (**EOG**), **Electroencephalography** (**EEG**) and **Electrocardiogram** (**ECG**) are widely used in clinical medication. Except for hardware chips, other computer-assisted prevalence of deep neural networks and machine intelligence, have provided great convenience for

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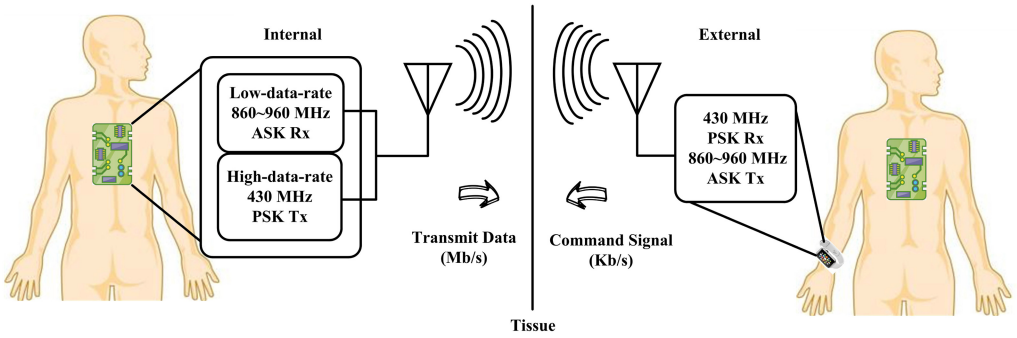


Fig. 1. Topology of a biomedical transceiver.

doctors to acquire the physical condition of patients [1, 7, 19–22, 25]. Considering the sensitivity of capturing these physiological data, most of the biomedical devices are implanted in the human body and need to transmit the data wirelessly through the human tissue, but to overcome the disturbance of human tissue during the transmission may lead to a huge power consumption [17]. As a result, transceivers with low-power solutions are needed. Moreover, these biomedical devices are generally powered by an internal lithium-ion battery, when the internal batteries of devices are exhausted, they need to be removed and replaced by surgery [4]. But the risk of infection during replacement is three times that of initial implanted, then these devices are required to be able to work at least for 10 years [3, 10]. Meanwhile, energy-efficient transceivers are worthwhile to extend the service life of the implanted biomedical devices.

The topology of a biomedical transceiver is depicted in Figure 1, as shown in Figure 1, for biomedical transceivers, data transmission is usually asymmetric [9]. At the downlink, the transceiver only needs to receive simple commands to control the operation of external devices, and the received data rate is low, about hundreds of Kb/s. However, the data collected by external devices (such as temperature sensors, pressure sensors, electrode array or cameras) are usually very large, resulting in a transmission data rate of several Mb/s. If a conventional symmetric topology is utilized, the energy efficiency will be inevitably low. And a new topology is demanded. Moreover, in order to prolong the service life of the device, a low power wireless transmitter is increasingly important due to a higher data transmission. Currently, state-of-the-arts focus on high-speed transmission. In [5], a transceiver for the **body-area network** (**BAN**) is introduced, which can transmit data at a peak rate of 1 Mb/s with the power consumption of 2.9 mW. In [15], a transceiver for neural recording was verified whose data transmission rate can reach up to 8 Mb/s and its total power consumption is 3.67 mW. In [16], a transmitter with two types of fractional-injection-locking techniques for multichannel transmission capabilities was presented, when the data rate is 11 Mb/s and the power consumption is 4.08 mW. The increasing data rate inevitably leads to an increase in power consumption. Moreover, with the continuous development of biomedical technology, there is a higher requirement for precise analysis of acquired physiological signals. As a result, the number of nerve electrodes that can be integrated into a biomedical microsystem has surged dramatically. In [2], a high-density electrode array with thin-film printing technology that can be used for cerebral cortex monitoring is proposed, with an electrode density up to 400 per square centimeter. In [18], a high-density electrode array integrated with ultra-thin and flexible silicon nanotransistors was verified to achieve high spatial resolution cerebral cortex sampling. In [8], an organic material-based, ultra-integrated, biocompatible and expandable neural interface array (the "NeuroGrid") was proposed whose electrode density can reach tens of thousands per square centimeter.

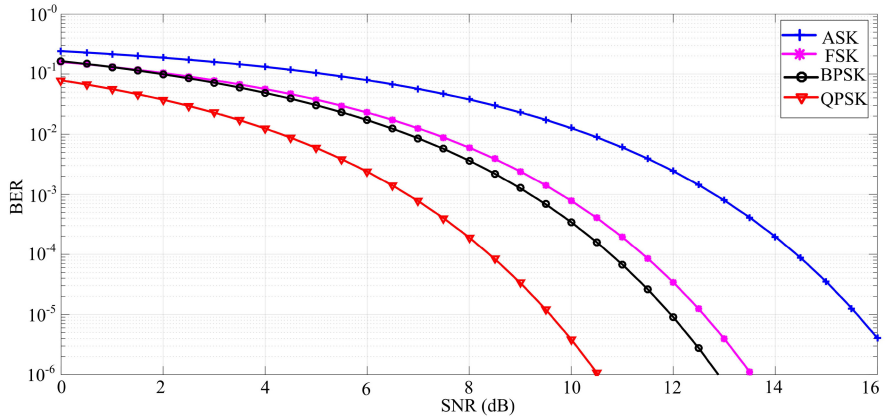


Fig. 2. BER comparison of ASK, FSK, BPSK, and QPSK.

The high-density electrode array makes it possible to realize high precision implantable devices targeted for neural applications. In [14], a closed-loop deep brain stimulator with a four-channel, 100 k sample/s sampling rate neural signal recording was introduced. In [12], an 8-channel neural signal recording front-end with 100 k sample/s sampling rate and 5-bit resolution for cerebral cortex, stimulation was verified. This high-resolution multi-channel neural recording signal directly improves transmission data rate. More specifically, the data rate is related to several parameters as shown in Equation (1).

$$Data.rate = channel.no \times sampling.rate \times bit.no. \tag{1}$$

Where channel.no is the number of channels, sampling.rate is the sampling rate of electrodes, and bit.no is the number of resolution bits. Suppose that the transmitter is designed for a neuroelectronic system with a maximum of 10 simultaneous recording channels, 100 k sample/s sampling rate and 10-bit resolution. According to Equation (1), the consequent transmission data rate up to 10 Mb/s is required.

Generally, modulation schemes used in low-power biomedical transceivers mainly include **amplitude-shift keying** (**ASK**), **frequency-shift keying** (**FSK**), and **phase-shift keying** (**PSK**), where PSK can be divided into **binary phase-shift keying** (**BPSK**) and **quadrature phase-shift keying** (**QPSK**). Figure 2 compares the **bit error rate** (**BER**) of ASK, FSK, BPSK, and QPSK modulation under different **signal-to-noise ratio** (**SNR**). As shown in Figure 2, PSK series has less bit error rate than both ASK and FSK at the same SNR. Besides, PSK requires only small bandwidth and can be extended to high-dimension modulation with an only phase difference, which is easily achieved in circuit design. Moreover, compared with BPSK, QPSK is equivalent to two orthogonal BPSK and can double the data rate under the same bandwidth. In addition, considering that the proposed modulator is aimed at biomedical devices, **intra-body communication** (**IBC**) with 64 MHz carrier is employed which uses the human body as the transmission medium. According to Moore's Law, the size of the logic circuits and power supply are reduced proportionally. The logic process is widely used in the integrated circuits due to its easy integration. Currently, the channel length of logic processes can be scaled to several nanometers, which are approximately near the size of a single atom. Consequently, the fabrication cost of the advanced logic processes can be only afforded by large companies. Figure 3 shows the general design methodology of logic circuits. The design flow in Figure 3 starts with the design specification. After architecture design, **register-transfer level** (**RTL**) coding, logic and physical synthesis, the circuit is laid out to be

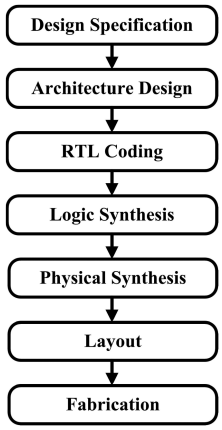


Fig. 3. General design methodology of logic circuits.

manufactured. In logic circuits, the transistors work as switches in saturation or cut-off regions. The current consumption is low in the cut-off region, but in the saturation region, the current consumption is not controlled and is usually very high. The dynamic power consumption of a logic switch can be depicted in Equation (2).

$$P_D = C_L \times V_{DD}^2 \times f. \tag{2}$$

Where $C_L$ is the equivalent load capacitance, $f$ is the operating frequency of the system, and $V_{DD}$ is the supply voltage. The circuit completes the state transition by charging and discharging the capacitance $C_L$. From Equation (2), the supply voltage is a quadratic term relative to the power consumption of the system. If the supply voltage can be reduced, the power consumption can be greatly reduced. But nowadays, modulators are consisting of fixed digital blocks provided by the foundry such as **Taiwan Semiconductor Manufacturing Company** (**TSMC**), **United Microelectronics Corporation** (**UMC**). Each single block is designed for general purpose and no special optimization on power is done. If these fixed blocks are used, they may degrade the performance, especially for power-hungry medical devices. Compared with expensive advanced logic circuits, analog circuits can be designed independently. Analog circuits can be customized and optimized to have better energy efficiency with some design skills such as subthreshold bias and lower supply line, it can be adjustable and exhibits flexibility compared with those blocks in **process design kit** (**PDK**) tools. The supply voltage can be lowered by 10% due to the headroom of the designated supply voltage, leading to a higher energy efficiency.

In this article, a new asymmetric topology is utilized to adapt to data rate requirements. Combining the advantages of both analog and digital circuits design, a quasi-digital QPSK modulator circuit is realized by pure analog circuits which follow a logic design flow. The system function is verified by simulation. In Section 2, the architecture and circuit design are described. In Sections 3 and 4, the simulation process and simulation results are given, respectively. And the final Section 5 provides the conclusion.

## 2 ARCHITECTURE AND DESIGN

Generally, the mathematical function of QPSK modulation can be indicated by Equation (3), where $b_m$, $b_{m+1}$ are coefficients of two sinusoid waves, respectively. As shown in Equation (3), $b_m$ and $b_{m+1}$ of two sinusoid waves can have a value of 1 or −1. After simple trigonometry, the modulation signal can be rewritten as Equation (4), where $k$ can equal to 1, 2, 3, and 4. As shown in Figure 4(a),

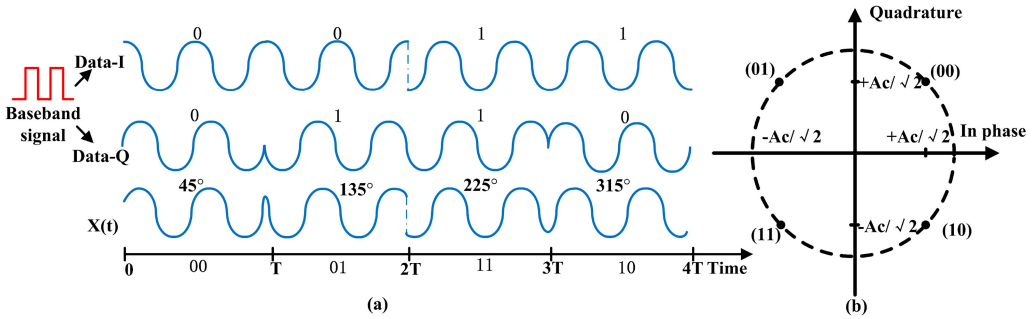


Fig. 4. (a) QPSK modulation diagram, (b) QPSK constellation diagram.

when the input data of the modulator is a binary sequence, the binary data is first divided into two paths, noted as Data-I and Data-Q, so as to match the phase of the quadrature carrier. These two paths are then combined into a 2-bits symbol, according to the value of $b_m$ and $b_{m+1}$. The 2-bits symbol has four combinations, where 00 corresponds to a phase of 45°, 01 corresponds to a phase of 135°, 11 corresponds to a phase of 225°, and 10 corresponds to a phase of 315°. The information is carried on the phase of the carrier implies that modulation can be easily realized by a phase selector to choose different quadrature signals. The amplitude in Equation (4) is normalized to 1 with ease of circuit implementation, regarding to the *Gnd* and $V_{DD}$. The normalized constellation diagram is mapped in Figure 4(b), according to the phase selection of the phase selector controlled by the baseband signal, four symbols are located in circular coordinate, respectively, with each 2-bits constituting a symbol.

$$x(t) = b_m A_c \cos \omega_c t + b_{m+1} A_c \sin \omega_c t, \tag{3}$$

$$x(t) = \sqrt{2} A_c \cos(\omega_c t + k\pi/4). \tag{4}$$

The design flow of the proposed modulator is shown in Figure 5. The carrier frequency can be either from an on-chip **phase-locked loop** (**PLL**) or off-chip crystal. The PLL can generate four quadrature-phase signals by internal quadrature oscillator directly. More general, the single-phase output is decomposed into four quadrature signals through a phase shifter, as shown in Figure 5. The baseband signal is divided into two paths Data-I and Data-Q by a serial-to-parallel converter. Last but not least, the Data-I and Data-Q baseband signals are multiplied by quadrature signals through phase selector, completing the modulation.

The corresponding overall architecture of the circuit is shown in Figure 6, which includes a carrier generator, a quadrature modulator and a serial-parallel converter. The carrier generator mainly includes a PLL and a phase shifter. The low-frequency reference clock is multiplied in PLL to obtain a higher frequency carrier signal. Then, a phase shifter is employed to convert the high-frequency carrier into four quadrature carriers with a phase difference of 90°. As for the serial-parallel converter, it is composed of a **demultiplexer** (**DEMUX**) unit to achieve decomposition of the baseband signal into two paths Data-I and Data-Q, according to the binary baseband data. The quadrature modulator contains two stages where the first stage is aimed at choosing two of the four quadrature signals, in the second stage, the retained channel-I and channel-Q are added in the waveform to obtain the final QPSK signal.

### 2.1 Serial-Parallel Converter

The binary baseband sequence needs to be combined into the 2-bits symbol to fulfil the modulation requirements. As shown in Figure 7, the method adopted here is using a DEMUX to split the data

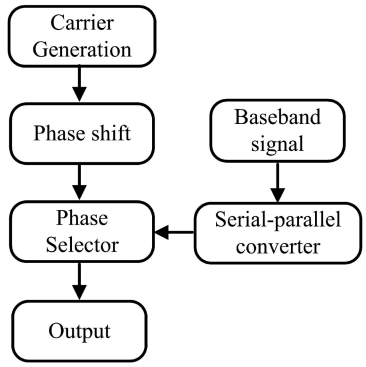


Fig. 5. Flow of the proposed modulator.

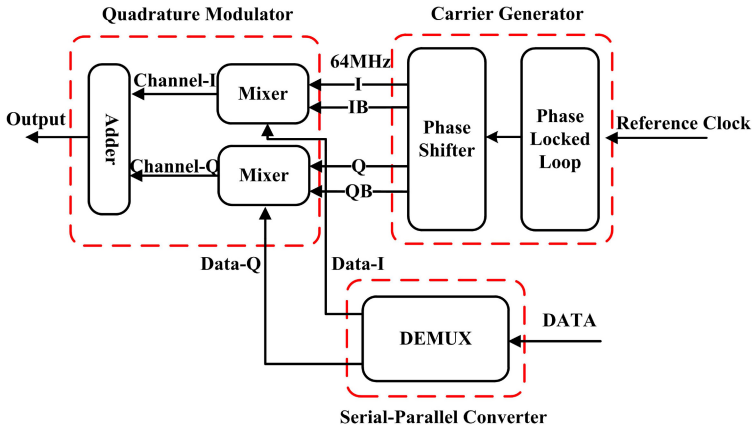


Fig. 6. Overall circuit architecture.

into two paths Data-I and Data-Q according to odd and even bits, a total of four combinations (00, 01, 10, and 11) is achieved. Resulting in that QPSK can transmit 2 bits of information in per modulation.

## 2.2 Carrier Generator

The carrier generator is one of the important components in the modulator. Its main function is to generate precise frequencies referred to as an outside crystal. As shown in Figure 8, the entire carrier generator is mainly composed of a PLL and a phase shifter. Where the PLL includes a **phase frequency detector** (**PFD**), a **charge pump** (**CP**), a **low pass filter** (**LPF**), a **voltage-controlled oscillator** (**VCO**) and an injection-locked frequency divider. The PFD compares the phase difference of feedback frequency $F_{FB}$ and reference frequency $F_{REF}$ to generate a phase error signals $U_P$ and $D_N$. The error signals are then converted into a voltage by a CP and filtered by a LPF to remove high-frequency noise to generate $V_{ctrl}$, thereby adjusting the output signal frequency of the VCO. When the phase difference between $F_{FB}$ and $F_{REF}$ is fixed, the loop will be locked, and the VCO outputs a periodic sinusoid signals whose output frequency is multiple of the crystal frequency. It is worth mentioning that the injection-locked divider in the PLL feedback loop is employed to achieve linear phase tracking and clean the control voltage of the charge pump, since

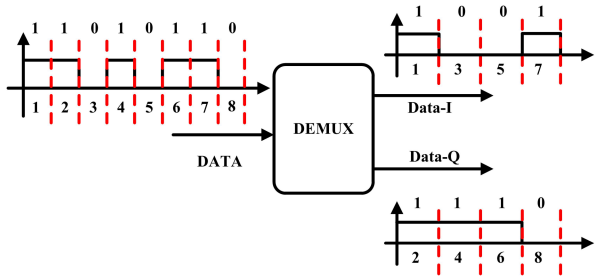


Fig. 7. Serial-Parallel converter.

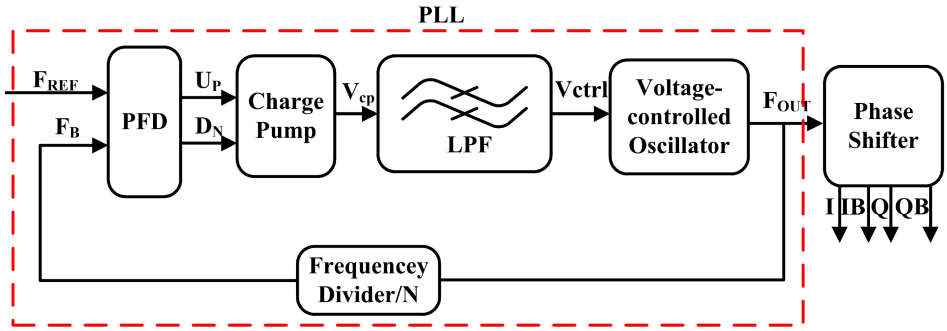


Fig. 8. Carrier generator.

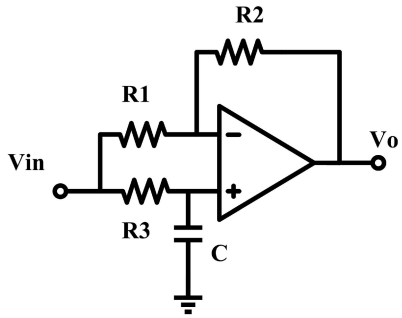


Fig. 9. All-pass filter.

the control voltage of the charge pump can increase in-band noise with a higher BER. According to the preset frequency dividing number $N$, the frequency divider can derive the output signal $F_{FB} = F_{OUT}/N$. Here we choose the reference signal $F_{REF}$ to be 8 MHz and $F_{OUT}$ to be 64 MHz.

The shifter consists of an all-pass filter and inverter. The output signal of the VCO is phase-shifted by 90° through an all-pass filter. Then the two signals with a phase difference of 90° are inverted by the inverter to obtain four signals with a phase difference of 90°. The all-pass filter adds phase shift (delay) to the response of the circuit, the mathematical deduction is as follows.

Equation (5) can be obtained from Figure 9, and Equation (6) is simplified from Equation (5).

$$\frac{\frac{1}{SC}}{R_3 + \frac{1}{SC}} V_{in} = \frac{R_2}{R_1 + R_2} V_{in} + \frac{R_1}{R_1 + R_2} V_o, \tag{5}$$

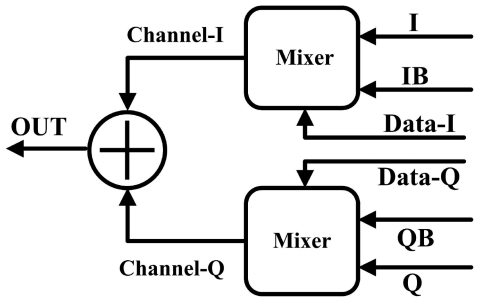


Fig. 10. Modulator architecture.

$$\frac{R_1 - SCR_3R_2}{1 + SCR_3} V_{in} = R_1 V_o. \tag{6}$$

When taking $R_1 = R_2 = R$ Equation (7) can be obtained.

$$\frac{V_o}{V_{in}} = \frac{1 - SCR_3}{1 + SCR_3} = e^{-j2\theta}. \tag{7}$$

Where $\theta = \arctan(2f\pi R_3 C)$, it can be seen that the output amplitude is not attenuated. When $f = 1/2\pi R_3 C$, the phase difference of the output signal is exactly 90° from the input phase.

### 2.3 Quadrature Modulator

The architecture of the quadrature modulator is redrawn here as shown in Figure 10. In Figure 10, the key block of the whole modulator is a Mixer-based phase selector, it directly selects two quadrature carriers in the in-phase path and the quadrature path. And the controlling signal is from the binary sequence, which is encoded into the differential format by a DEMUX. Here, the Mixer and Adder need to be carefully designed as the delay time of Mixer and Adder may arise to random phase and frequency deviation, leading to a deteriorated BER.

### 2.4 Signal Demodulation

In order to facilitate the simulation, a coherent demodulation scheme is adopted. Figure 11 shows the process of coherent demodulation. The QPSK signal is divided into two channels and two LPF are set in the orthogonal channel to obtain $I(t)$ and $Q(t)$, the baseband data can be recovered by level judgment and serial-parallel conversion, the mathematical deduction is as follows.

The received signal through the channel can be expressed in Equation (8).

$$S_{QPSK}(t) = I(t)A\cos(2\pi ft) + Q(t)A\sin(2\pi ft). \tag{8}$$

Where $I(t)$ and $Q(t)$ are the in-phase and quadrature branches, respectively, and $f$ is the carrier frequency. The in-phase branch and the orthogonal branch can be obtained in Equations (9) and (10), respectively.

$$\begin{aligned} I_i(t) &= S_{QPSK}(t)\cos(2\pi ft) \\ &= [I(t)\cos(2\pi ft) + Q(t)\sin(2\pi ft)]\cos(2\pi ft) \\ &= I(t)\cos^2(2\pi ft) + \frac{Q(t)\sin(4\pi ft)}{2} \\ &= \frac{I(t)}{2} + \frac{I(t)\cos(4\pi ft)}{2} + \frac{Q(t)\sin(4\pi ft)}{2}, \end{aligned} \tag{9}$$

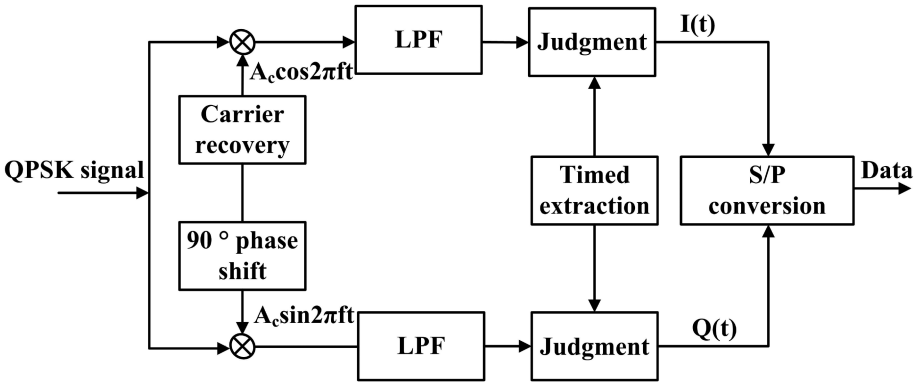


Fig. 11. Coherent demodulation.

$$\begin{aligned} Q_q(t) &= S_{QPSK}(t)\sin(2\pi ft) \\ &= [I(t)\cos(2\pi ft) + Q(t)\sin(2\pi ft)]\sin(2\pi ft) \\ &= Q(t)\sin^2(2\pi ft) + \frac{I(t)\sin(4\pi ft)}{2} \\ &= \frac{Q(t)}{2} + \frac{I(t)\sin(4\pi ft)}{2} - \frac{Q(t)\sin(4\pi ft)}{2}, \end{aligned} \tag{10}$$

$$I_i(t) = \frac{I(t)}{2}, \tag{11}$$

$$Q_q(t) = \frac{Q(t)}{2}. \tag{12}$$

The filtered signal can be represented by Equations (11) and (12), so the original data are obtained.

### 2.5 Noise Model

To verify the characterization of modulator performance to noise, we carry out the modeling of the noises. Generally, different noise violations can be generalized into frequency-domain phase noise that could cause the time-domain jitter of the signal. The circuit non-linearity due to the random phase uncertainty will significantly increase the bit error rate. In general, phase noise is modeled as a Wiener process (integration of a Gaussian random process) [23]. The bit error rate $P(e)$ of the QPSK system with intrinsic phase noise is given by Equation (13), where $P_b\{e|\theta(k) = \varepsilon\}$ is the bit error rate when the phase noise equal to $\varepsilon$; $p_{\theta(k)}$ is the phase noise probability density function. The phase noise probability density of the carrier generated loop conforms to the Tikhonov distribution, as shown in Equation (14).

$$P(e) = \int_{-\pi}^{\pi} P_b\{e|\theta(k) = \varepsilon\} \bullet p_{\theta(k)} d\varepsilon, \tag{13}$$

$$p_{\theta(k)}(\varepsilon) = \frac{\exp(\alpha\cos(\varepsilon))}{2\pi I_o(\alpha)}. \tag{14}$$

Where $I_0(\alpha)$ is a modified zero-order Bessel function, and $\alpha$ is the signal-to-noise ratio of the carrier generator loop. When $\alpha$ is » 1, $\alpha^{-1}$ is close to the phase noise variance. The next step is to

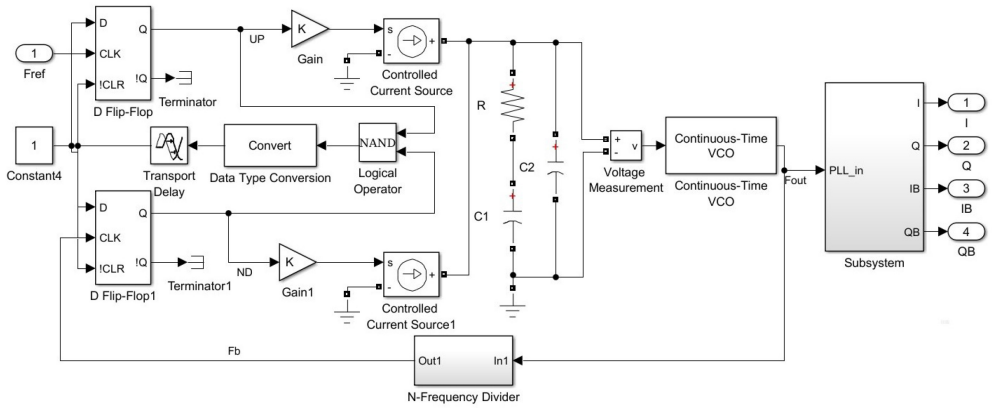


Fig. 12. Carrier generator.

define $P_b\{e|\theta(k)=\varepsilon\}$. As the system signal-to-noise ratio is $E_b/N_o$, the derivation process of the $P_b\{e|\theta(k)=\varepsilon\}$ is given in [23], which can be simplified in Equation (15).

$$P_b(e) \approx \begin{cases} \frac{1}{2\sqrt{\pi}} \exp\left\{-\frac{E_b}{N_o}\left(1-\frac{2E_b}{\alpha N_o}\right)\right\} + \tilde{P_b}(e) & \frac{E_b}{N_o} < \alpha \\ \frac{1}{2}\left[\sqrt{\frac{\alpha}{\pi}}\right]\left(\frac{E_b}{N_o}\right)^{\frac{1}{2}} \bullet \exp\left\{-\alpha\left(1-\frac{1}{\sqrt{2}}\right)+\frac{\alpha^2}{16(E_b/N_o)}\right\} + \tilde{P_b}(e) & \frac{E_b}{N_o} \geq \alpha. \end{cases} \tag{15}$$

Where $\tilde{P_b}(e)$ is the bit error rate caused by phase noise, it can be obtained by Equations (16) and (17). In Equation (17), $I_n(\alpha)$ is a modified $n$-order Bessel function.

$$\tilde{P_b}(e) \approx \frac{1}{2}\left\{F_\alpha\left(\frac{\pi}{4}\right) + F_\alpha\left(\frac{3\pi}{4}\right)\right\}, \tag{16}$$

$$F_\alpha(\beta) = 2\int_\beta^\pi p_{\theta(k)}(\varepsilon)d\varepsilon = 1 - \frac{\beta}{\pi} - \frac{2}{\pi}\sum_{n=1}^{\infty}\frac{I_n(\alpha)\sin(n\beta)}{nI_o(\alpha)}. \tag{17}$$

## 3 CIRCUIT SIMULATION

### 3.1 Carrier Genertor

As discussed in Section 2, the corresponding circuit of the carrier generator is shown in Figure 12. The whole block functions as a PLL. As shown in Figure 12, two D-type flip-flops, a NAND gate and a Transport Delay block constitute a PFD, a data type conversion block is used here for signal matching. As for input ports, $F_{REF}$ is the input signal, $F_B$ is the feedback signal of the frequency divider, $U_P$ and $D_N$ are charge and discharge control pulse of the charge pump, respectively. Since the carrier signal frequency is selected as 64 MHz, according to the analysis in Section 2, the dividing number $N$ is retained to 8. Two controlled voltage sources and two gain units constitute the charge pump which can be adjusted by setting the gain $K$. The VCO used in the library has a voltage gain $K_{VCO}$ of 64 MHz/V. Followed by the charge pump is a passive second-order LPF realized by an $R$, $C_1$, and $C_2$ parallel network. From mathematical model point of view, the inherent integral characteristics of the VCO contributes a pole to the open-loop transfer function, consequently, this PLL behaves as a third-order loop. Compared with the second-order PLL with a first-order filter composed of only $R$ and $C_1$, the third-order loop may have stability problems if the phase margin is not enough. As far as stability is concerned, by setting that $C_2$ is one-tenth to $C_1$, the closed-loop frequency response can keep relatively stable [13].

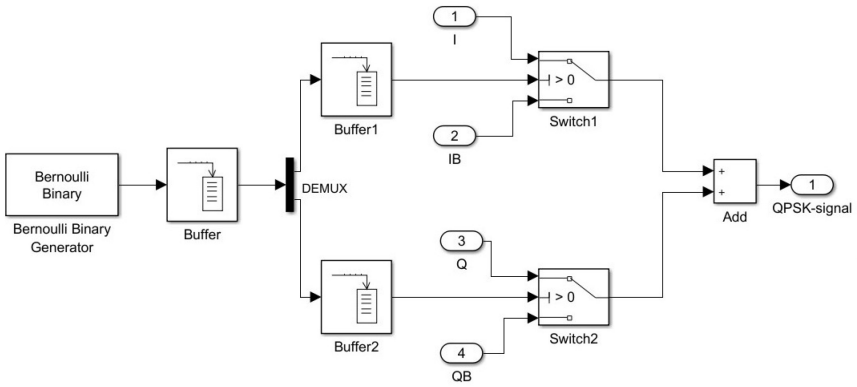


Fig. 13. Quadrature modulator.

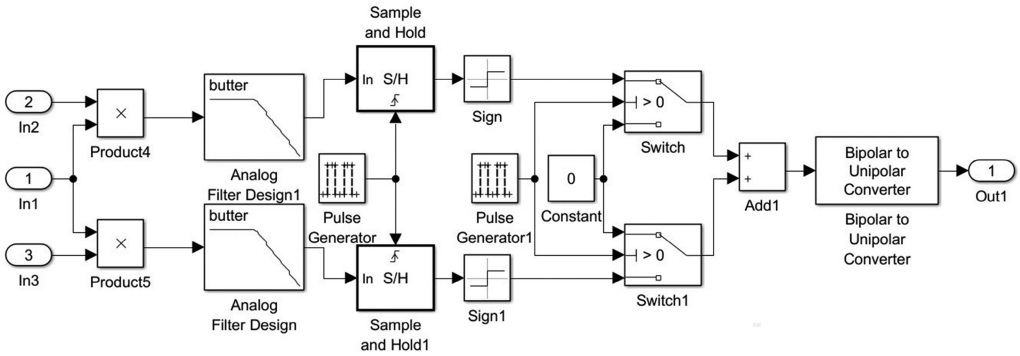


Fig. 14. Coherent demodulation.

### 3.2 Quadrature Modulator

The quadrature modulator is shown in Figure 13, where a Bernoulli Binary Generator is used to generate the random binary data. The other four input ports are quadrature carrier signals I, IB, Q, and QB, respectively. Three buffers play the role of buffering and transmitting data, and the DEMUX block encodes the baseband signal differentially. Two logic switches with single-ended output select one of the two carrier phases, when the encoded data is logic 1, the switch selects carrier I or carrier Q, when the differential code is logic 0, the switch selects carrier IB or carrier QB. Finally, the two modulated signals are added by an adder to obtain the QPSK signal. Through the simulation, some simple blocks still need to be taken into consideration, as the delay time of adders and mixers severely affect the accurate phase.

### 3.3 Demodulation

According to the analysis of the Section 2, the coherent demodulation block shown in Figure 14 is constructed. As shown in Figure 14, the received QPSK signal is divided into two channels, and orthogonal carriers are used to demodulate the received signal. Then, the demodulated signal enters the delay decision passing through the low-pass filter and the sample-and-hold block to obtain a parallel binary sequence. Sign delay is a hysteresis comparator, which plays the role of sampling decision. After the signed judgment, stable binary sequences can be obtained. Finally, the

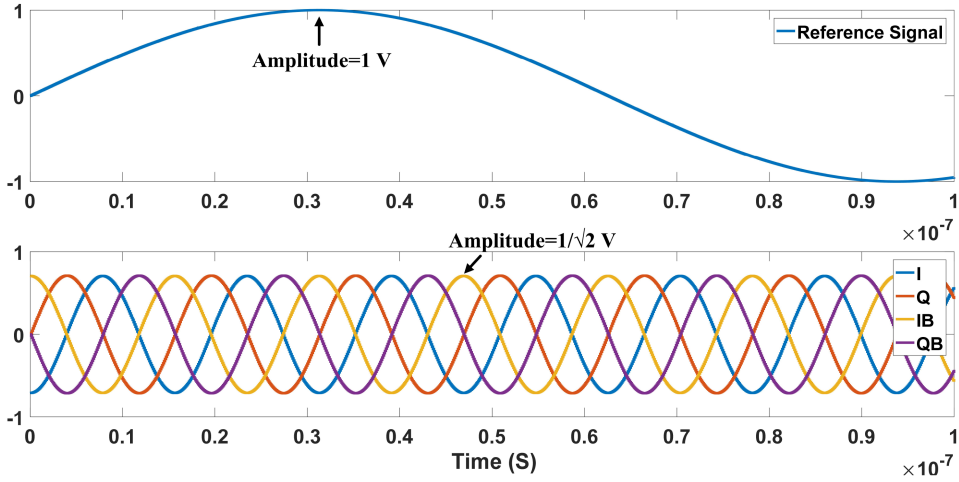


Fig. 15. Simulation of the carrier generator.

baseband signal can be obtained by timing extraction and parallel-serial conversion of the binary sequences.

## 4 SIMULATION RESULTS

According to the design requirements, the second-order filter is preset to $R = 2.3K\Omega$ , $C_1 = 22.5$ pF, and $C_2 = 1.5$ pF. The relative simulation results of carrier generation are shown in Figure 15, where the reference signal is a sinusoidal signal with the amplitude of 1 V, the time span of $X$-axis is limited to 100 ns and the frequency can be calculated to 8 MHz, the frequency of four output quadrature signals downwards is eight times of reference frequency with a value of 64 MHz. In order to make the output amplitude of the final QPSK signal equal to 1 V, the carrier amplitude is generalized to $1/\sqrt{2}$ V. Figure 15 verifies that after the output phase of the VCO is adjusted by the phase shifter, and four quadrature signals with a phase difference of 90° can be obtained.

Figure 16 shows the baseband signal modulation procedures, from bottom to top view of Figure 16, there are Data-Q, channel-Q, Data-I, channel-l, and QPSK signal in sequence, where channel-l, Data-I is the modulated signal and baseband signal of the in-phase path, channel-Q, Data-Q is the modulated signal and baseband signal of the quadrature path. The phase of the carrier in channel-I/Q is reversed by 180° according to the baseband signal, and the amplitudes of modulated signal channel-I and channel-Q are both normalized to $1/\sqrt{2}$ V, when the two modulated signals of channel-I and channel-Q are added together, the final QPSK signal will have 1 V amplitude with ease of circuits implementation. Hereby, the symbols 11, 10, 00, and 01 of the QPSK signal are reflected in the phase of the final output signal. However, this inherent phase discontinuity may deteriorate the bit error rate. The modulation data rate can be calculated from Equation (18).

$$D_r = \frac{1}{T} \times \log_2^M . \tag{18}$$

Where $M$ is a factor number, and $T$ is the period of the carrier. When $M$ equal to 4 in QPSK and $T$ is 200 ns; therefore, the data rate is 10 Mb/s, as shown in Figure 16.

The output spectrum is shown in Figure 17. With the carrier frequency of 64 MHz, and modulated signal demonstrates two sidebands with a power of ± 19.64 dBm. Since the QPSK modulation is achieved by upconverting the baseband signal frequency to the carrier frequency through the

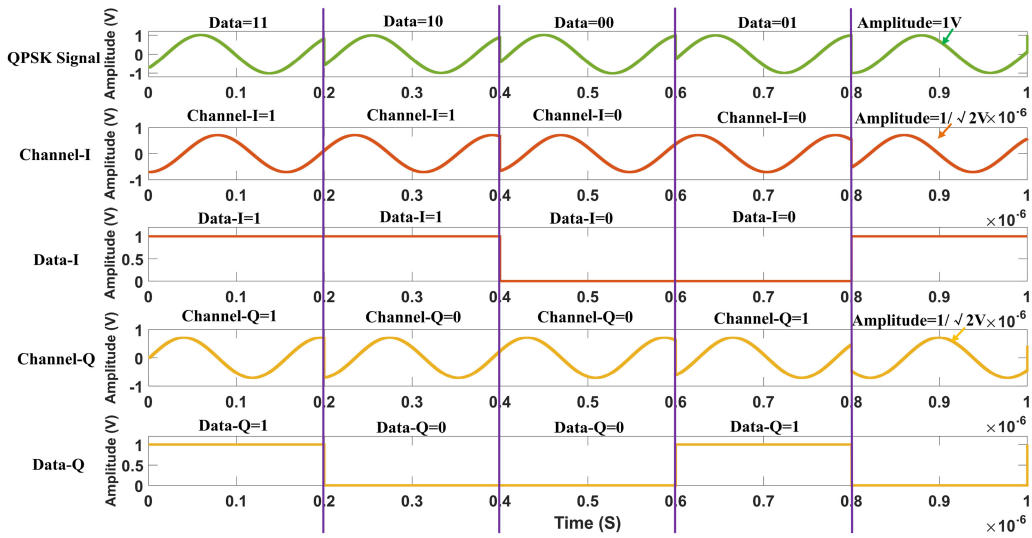


Fig. 16. QPSK modulation simulation.

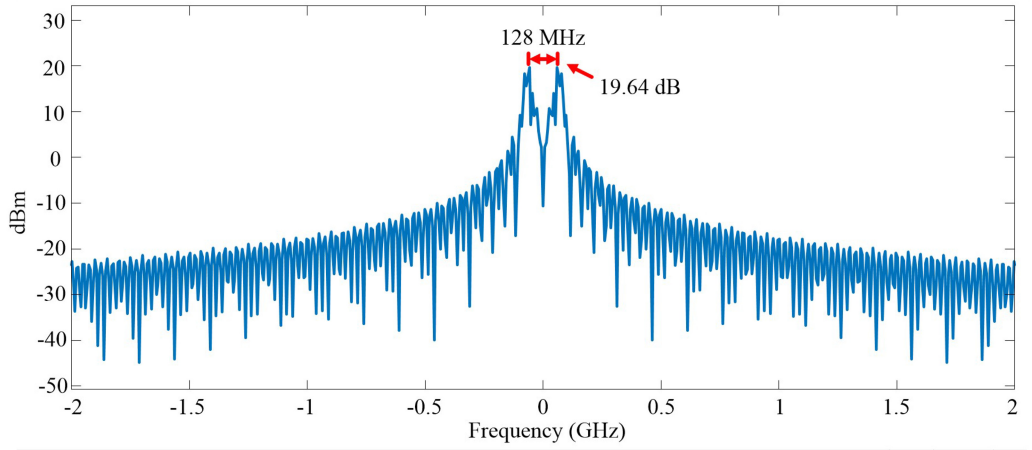


Fig. 17. QPSK signal spectrogram.

multiplication of the carrier signal and the baseband signal, the Fourier series of this modulator output contains both carrier and baseband spectral information. Resulting in that the frequency interval is 128 MHz. When the channel SNR equals to 10 dB, the constellation diagram can be attained in Figure 18(a), if the phase noise is taken into consideration, the constellation diagram is mapped in the Figure 18(b) based on Equation (13). In Figure 18(a) and (b), the $X$-axis is the amplitude of the in-phase signal (Data-I), while the $Y$-axis is the amplitude of the quadrature signal of (Data-Q), the red cross marks the ideal reference point. Figure 18(a) shows that white Gaussian noise causes the random phase of the signal, the signal phase shift is worsened when the phase noise is added in. The locus of the Figure 18(a) and (b) basically located around the reference point, which indicates that these signals still maintain the phase and amplitude characteristics of the baseband signal.

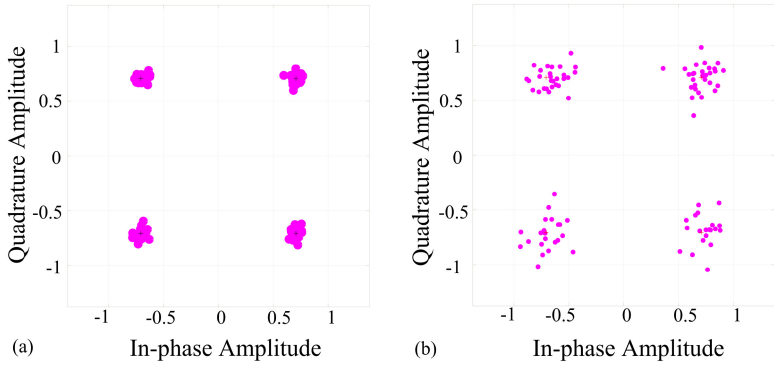


Fig. 18. Constellation diagram. (a) Constellation diagram with white Gaussian noise, (b) Constellation diagram with phase noise.

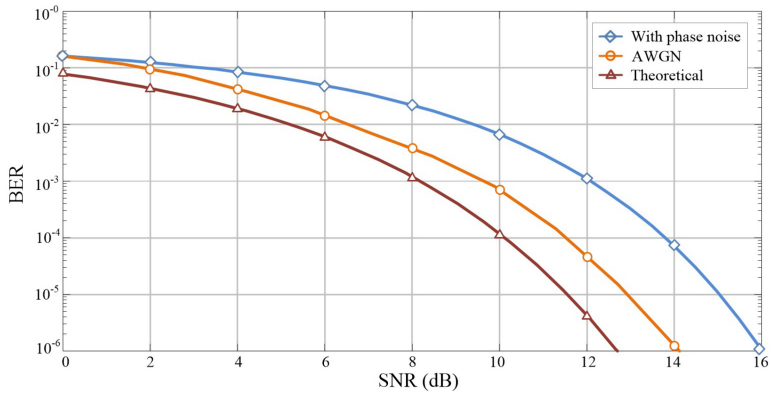


Fig. 19. BER comparison.

By setting SNR, the BER under different conditions can be obtained. When the frequency of the carrier is set to 64 MHz, and the data rate is 10 Mb/s, the Figure 19 can be obtained. Figure 19 shows the BER under white Gaussian noise and phase noise disturbances. It can be seen from Figure 19 that compared with the theoretical analysis without any noise, the modulator achieves a BER better than $10^4$ under white Gaussian noise disturbance if the SNR is set at 12 dB, but the BER just drops to $10^3$ with phase noise under the same situation. Figure 19 demonstrates that even an optimal energy-efficiency aforementioned is achieved, there is still a tendency toward a trade-off between BER performance and power consumption in further design. Literature comparison is shown in Table 1. As shown in Table 1, reference [6] can achieve a bit error rate of $10^7$ but at the cost of higher power consumption. The digital PSK modulation used in [11] and [24] does not perform as well as the proposed modulator in terms of bit error rate. From Table 1, it is obvious that our energy consumption per bit is 50 pJ/b, which is significantly superior to the previous work. Since the power consumption has always been a bottleneck restricting the development of biomedical devices, this experiment shows that the customized analog circuits exhibit the prospect of power reduction in nowadays digital modulation. Thanks to the analog nature of the proposed modulator, a relatively low power consumption is achieved.

Table 1. Literature Comparison

| Parameters | This work | Ding et.al [6] | Li et.al [11] | Zhang et.al [24] |
|---|---|---|---|---|
| Method | Analog | Digital | digital | digital |
| Modulation | QPSK | FSK | GPSK | F-OOK |
| Frequency | 64 MHz | 5 GKz | 2.4 GHz | 2.4 GHz |
| Data Rate | 10 Mb/s | 50 Mb/s | 1 Mb/s | 5 Mb/s |
| BER | $10^{-4}$ | $10^{-7}$ | $10^{-6}$ | $10^{-6}$ |
| Energy/bit | 50 pJ/b | 136 pJ/b | 940 pJ/b | 1.22 nJ/b |
| Power Consumption | 0.5 mW | 6.8 mW | 0.94 mW | 6.1 mW |

## 5 CONCLUSION

This article presents a quasi-digital QPSK modulator design implemented by analog circuits. The system function is verified by MATLAB/Simulink. The entire system with simplicity only includes a carrier generator, a quadrature modulator and a serial-parallel converter, leading to a lower power consumption. The carrier generator can generate a 64 MHz stable phase quadrature signal with the 8 MHz reference input. When the data rate is 10 Mb/s and the SNR of the Gaussian channel is 14 dB, it can still maintain a BER below $10^4$. When the SNR is 10 dB, it can be seen from the constellation diagram that most signals still retain the original characteristics with low bit errors. This architecture is especially suitable for biomedical devices and is also promising for some energy-efficient hardware designs.

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